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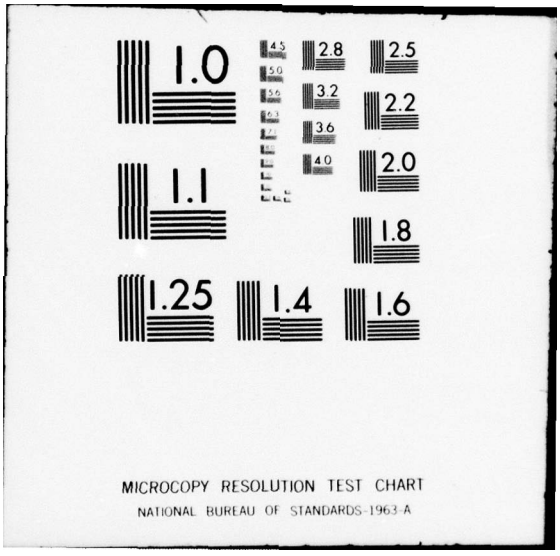
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(10) BY S.A. POWERS AND J. ST. AMAND

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The primary and secondary mass storage subsystems of the DP&D subsystem of TACC Automation are examined from the standpoint of hardware response to software commands.

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1.0 GENERAL DESCRIPTION

1.1 Introduction

This document addresses the characteristics of the mass storage subsystems of the Data Processing and Display Subsystem (DP&D) of the Tactical Air Control Center Automation program (TACC Automation) from the perspective of computer programs. The mass storage requirements of the DP&D are satisfied by two subsystems: the Primary Mass Storage Subsystem (PMSS) stores data on disks while the Secondary Mass Storage Subsystem (SMSS) employs magnetic tapes for storage of data.

This document, otherwise defined as an Equipment Characteristics Manual (ECM), has been written to serve as an aid for software specialists - these might be Air Force personnel or civilian contractors - responsible for the development or maintenance of computer programs associated with the DP&D.

Section 2 provides background information on the various hardware elements of the DP&D which are involved in the transfer of data to and from the DP&D's mass storage subsystems. Section 3 provides detailed information on the means of transferring data to and from the PMSS while Section 4 provides similar information for the SMSS.

To provide a user with a single source document, the bulk of the material assembled here is taken from other sources. It is hoped that the consolidation of materials will prove to be one of the more useful features of the ECM.

A further motivation for an ECM is that of providing the programmer with a document that transcends hardware boundaries. Both the PMSS and SMSS incorporate several pieces of equipment provided by different manufacturers. While documentation is readily available for each item separately, no document informs the programmer as to how the elements work together. It is our hope that this document reduces the extent of this problem.

1.2 The Rationale for an ECM

During the creation of TACC Automation Package I DP&D computer programs, the need for a comprehensive description of the TACC Automation system equipment was much in evidence. The consensus was that the creation of Package II programs that would exploit the full potential of TACC machinery would be most efficiently accomplished via an authoritative description of machine characteristics.

1.3 The Scope of the ECM

The topics selected for inclusion in this ECM and the depth of coverage provided was determined by considering the needs of the intended user. This document is written for an experienced software specialist with little or no experience with the mass storage subsystems of the DP&D subsystem. As the user gains experience, the value of this document decreases. This is consistent with our decision to write a document that did not impose or imply computer program discipline. The choice of methods for machine utilization for achieving optimum TACC system performance is properly a task for the system programmers.

The ECM is intended to provide the user with information - not readily available from other sources - necessary to accomplish the successful and efficient transfer of data to and from the Primary and Secondary Mass Storage Subsystems of the DP&D. As sufficient documentation is currently available on the DP&D's AN/UYK-7 computer and its input/output controller, it will be assumed that the user is already familiar with their operation and programming. The user is referred to Reference 1 for a basic description of the AN/UYK-7 and its I/O controller; to Reference 2 for detailed information on the operation and programming of the I/O controller; and to Reference 3 for a detailed manual of the AN/UYK-7 assembly language.

2.0 THE COMPUTER SUBSYSTEM

The units of the DP&D's mass storage subsystems provide for the storage of data transferred from the DP&D's Computer Subsystem and for the retrieval of this data for transfer back to the Computer Subsystem. It is apparent, then, that a proper understanding of the functioning of the mass storage subsystems requires familiarity with the elements of the Computer Subsystem which participate in the transfer of data to and from mass storage. These Computer Subsystem components are:

a. 1 Data Processor Computer (DPC)

b. 2 Error Detection Units (EDU)

c. 2 Peripheral Controller Units (PCU)

A block diagram of the DP&D's Computer Subsystem and mass storage subsystems is given in Figure 2.1.

2.1 The Data Processor Computer

The Data Processor Computer (DPC) is a Univac AN/UYK-7 Computer Set. The elements of the DPC which are involved in the data transfer process are:

a. 2 Central Processor Units (CPU)

b. 6 Memory Units (MU)

c. 2 Input/Output Controllers (IOC)

d. 2 Input/Output Adapters (IOA)

The two CPUs are operated in a dual processor configuration where one CPU serves as an on-line spare, or backup, to the other active CPU. With this configuration, normal data processing functions can be maintained in the event that one CPU fails. However, the two CPUs can be operated in a multiprocessing configuration where the load of the data processing functions is shared by both CPUs if such a configuration becomes a requirement in the future.

Each CPU uses a computer word size of 32 bits and can address a total of 262K words (8×10^6 bits) of core memory. Each CPU has an average instruction execution time of 2.1 microseconds. The basic

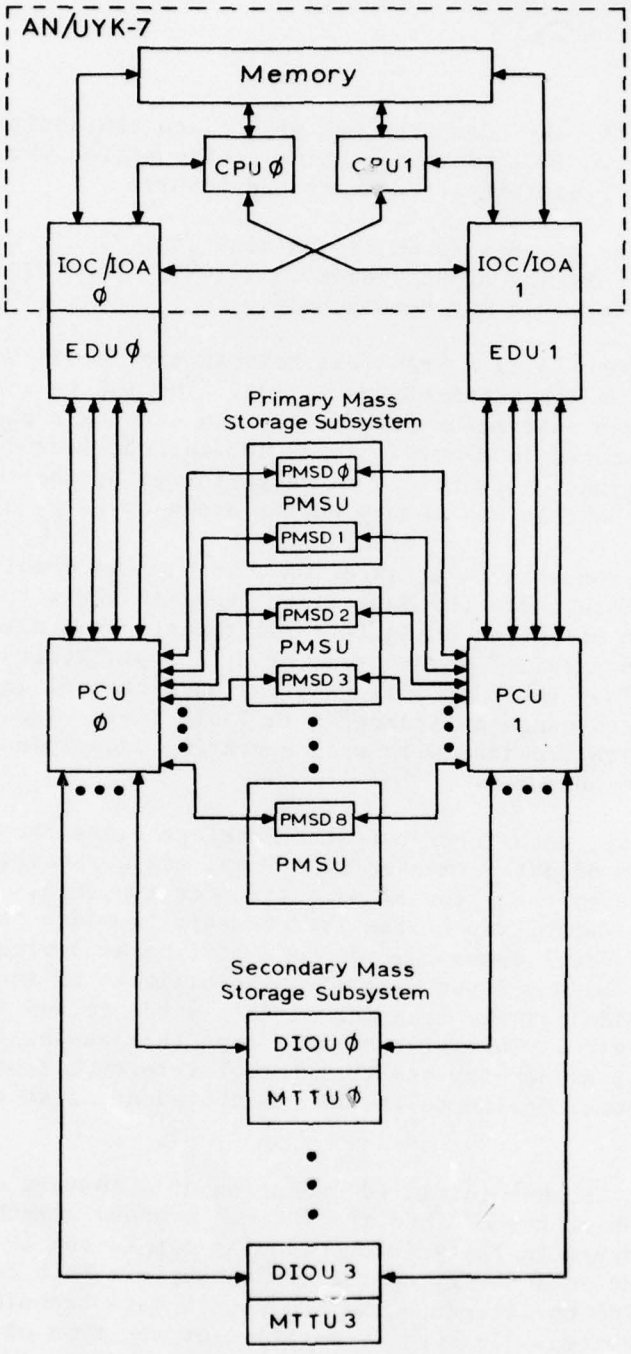


Figure 2.1 The DP&D's Computer And Mass Storage Subsystems

design of the AN/UYK-7 Computer Set will allow the addition of one CPU and up to two IOCs to the existing configuration with the incorporation of additional cabinets and modules.

Each of the six Memory Units contains 16K, 32-bit words for a total storage capacity of 96K words (3×10^6). Each CPU can execute instructions stored in any Memory Unit.

An IOC controls data transfers between the Memory Units and the input and output data channels of an IOA. The IOC is a programmable unit which, upon initiation from a CPU, can execute a chain of IOC instructions stored in Memory. These IOC instructions define the type of data transfer functions to be performed by the IOC and the input/output channels and memory buffer areas to be used.

Each IOC connects to a fixed IOA. The IOA is a multiplexing device which interfaces the data lines from the IOC with a set of 16 full-duplex input/output channels. All transfers of data are performed in a parallel word format of 8, 16, or 32 bits, plus one parity bit. The number of bits used for each channel is determined by its allocated usage as indicated in Table II-1. Two IOC/IOA combinations are provided with each operating independently under the control of the CPUs.

In general, each input/output channel provides the capability for four types of data transfer functions, and a specific IOC command initiates each type of data transfer function. The external function (EF) capability of the I/O channels provides for the transfer of control command words to a peripheral device. The output data (OD) and input data (ID) capabilities of the I/O channels provide for the transfer of data words to and from a peripheral device. The external interrupt (EI) capability of the I/O channels provides for the transfer of interrupt status words from a peripheral device to the DPC in the event of an error condition.

Once the CPU has initiated execution of a command chain by an IOC, operation of the CPU and the IOC can proceed asynchronously. A monitor interrupt facility is provided to enable the CPU to monitor the data transfer activity on the I/O channels. This facility permits the IOC to interrupt the CPU when a data transfer function has been completed. The CPU is notified of the type of function which has been completed (EI, EF, OD, or ID) and the I/O channel on which it was performed.

TABLE II-1

I/O CHANNEL ALLOCATION

CHANNEL NO. (DECIMAL)	ALLOCATION	DATA BITS
15	EDU	16
14	PCU (DISK)	32
13	PCU (TAPE)	16
12	PCU (DISK)	32
11	PCU (TAPE)	16
10	GROWTH	32
9	DISPLAY CONTROLLER	16
8	WRAP AROUND	16
7	WRAP AROUND	32
6	DISPLAY CONTROLLER	16
5	COMMUNICATIONS PROCESSING COMPUTER GROUP	16
4	DP&D STATUS PANEL	8
3	GROWTH	16
2	GROWTH	16
1	GROWTH	16
0	GROWTH	16

A single IOC can be used to control several I/O operations simultaneously through the activation of several IOC command chains in that IOC. In this event, it is possible for several requests for initiation of data transfer functions to be pending in the IOC at the same time either on the same channel or on different channels. To resolve such conflicting requests, a priority system is used in the IOC. Priority for data transfer requests is established first by channel (with channel 15 having highest priority and channel 0, the lowest) and secondly by function type (where the order of decreasing priority is EI, EF, OD, and ID).

When several chains are active in an IOC, several requests for monitor interrupts may be pending in an IOC simultaneously. Conflicting requests for monitor interrupts are resolved by the IOC using the same priority scheme used for servicing data transfer requests.

A complete description of the Data Processor Computer can be found in Reference 1 and a detailed discussion of the operation and programming of the IOC is provided in Reference 2.

2.2 The Error Detection Unit

An Error Detection Unit (EDU) built by General Dynamics is connected to each IOC/IOA pair. The EDU generates a parity bit for each word transferred out of the IOA on each I/O channel and checks for parity errors on each word transferred into the IOA on each I/O channel. Odd parity is used for normal activity on all channels. The EDU can, however, be programmed to generate even parity to permit testing the parity error detection capability of peripheral devices.

2.3 The Peripheral Control Unit

A Peripheral Controller Unit (PCU) is used to control the transfer of data between the Input/Output channels of an IOA and the units of the Primary and Secondary Mass Storage Subsystems. Each PCU is an identically tailored version of the Microprogrammable Processor (MPP) built by Control Data Corporation and executes a microprogram developed for use in the DP&D peripheral control application. Each PCU connects to a particular IOC/IOA of the DPC through four separate input/output channels. These channels are allocated as follows:

a. Two full duplex channels for primary mass storage with 32 bits plus parity in parallel per channel.

b. Two full duplex channels for secondary mass storage with 16 bits plus parity in parallel per channel.

Each PCU is connected to the Primary and Secondary Mass Storage Subsystems through a set of input/output channels as follows:

a. 10 Primary Mass Storage channels (Serial). (One channel is not in use in the First Article Hardware.)

b. 4 Secondary Mass Storage Channels (8 bits plus parity in parallel).

The PCU operates under the direction of control commands received from the DPC. Control commands received on the 32-bit channels are interpreted as disk commands; control commands received on the 16-bit channels are interpreted as tape commands. The PCU controls the output to Mass Storage devices of data words received from the DPC and input from Mass Storage devices of data words to be transferred to the DPC. The PCU monitors the operation of the Mass Storage devices and can transmit interrupt status words to the DPC reporting error conditions detected.

The functional relationships existing between the DPC, the PCU and the mass storage subsystems are as illustrated in Figure 2.2.

A single PCU is capable of handling the following simultaneous functions:

a. Data transfer to/from two disk units.

b. Data transfer to/from two magnetic tape units.

c. Control of two magnetic tape units performing functions not involving data transfer, e.g., rewind.

When both PCUs are being operated under load sharing, four disk units and four magnetic tape units can simultaneously exchange data with the DPC through the two PCUs.

A PCU is placed in an initial state with respect to its operation as a disk and tape controller in response to any of the following three events:

a. Power on of the PCU.

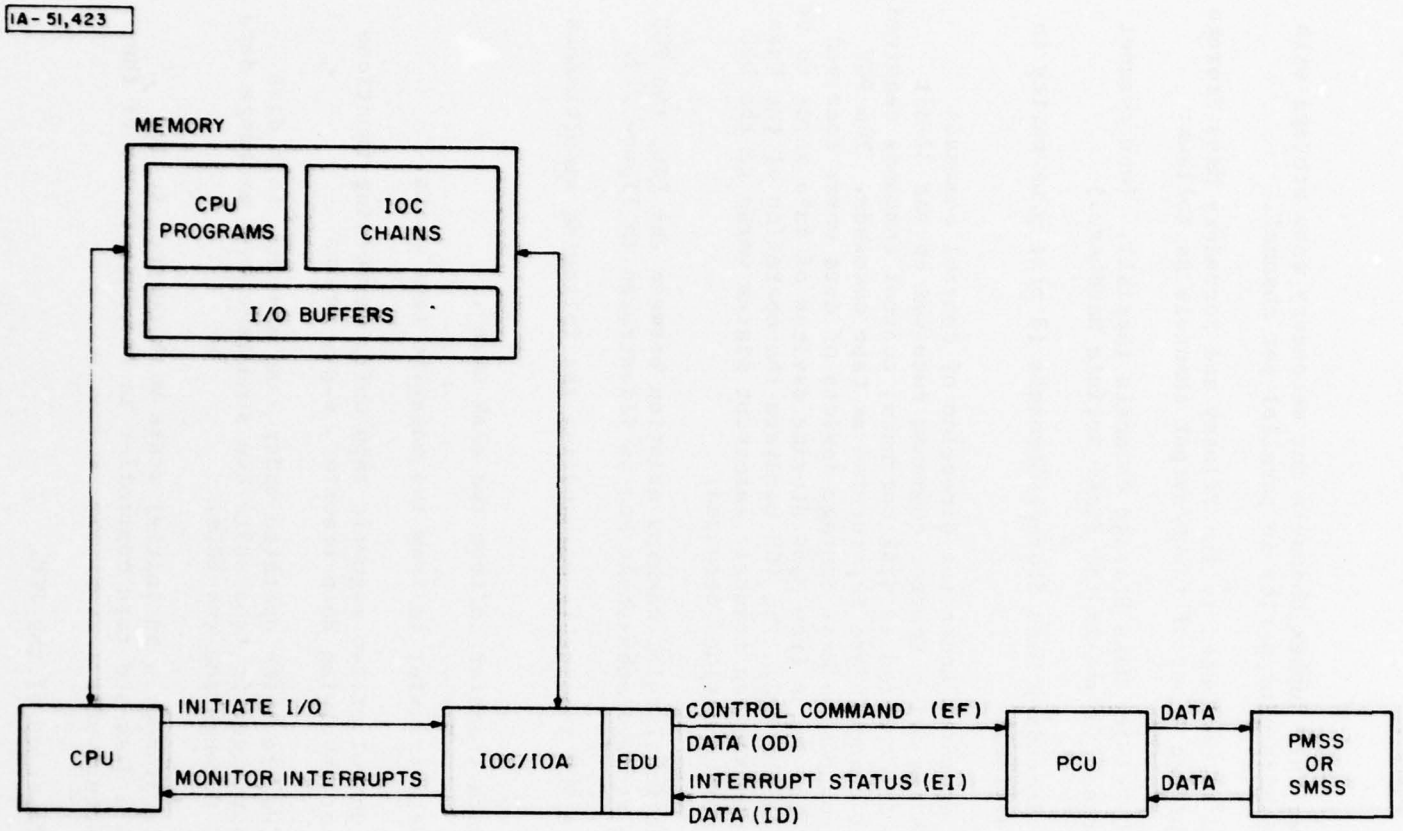


Figure 2.2 PMSS(SMSS)/COMPUTER SUBSYSTEM INTERFACES

b. Receipt by the PCU of a Master Reset PCU control command on either of the PCU's two tape data transfer channels. (This 16-bit command has the value 21400 .)

c. Depression of the Master Reset button on the PCU.

The significant characteristics of the PCU's initial state are noted in Sections 3.0 and 4.0.

3.0 THE PRIMARY MASS STORAGE SUBSYSTEM (PMSS)

3.1 Introduction

Three types of data transfer operations are provided for interaction between the DPC and the PMSS. The PCU, operating under the direction of commands received from the DPC, serves as the data transfer control interface between the DPC and the PMSS. A WRITE operation consists of the transfer of a block of data from memory to a disk unit. A READ operation consists of the transfer of a block of data from a disk unit to memory. A COMPARE operation consists of comparison by the PCU of a block of data transferred to the PCU from memory with a block of data transferred to the PCU from a disk unit. These three disk operations are elaborated upon in Section 3.4. Either PCU can be selected to serve as the interface for any disk unit of the PMSS upon command from the DPC. At any given time, however, at most one PCU can be selected for control of a particular disk unit.

A PCU can initiate a data transfer operation for any disk unit under its control upon command from the DPC. The PCU controls the necessary transfer of data words to or from the disk unit and monitors the performance of the transfer operation. The particular disk monitoring capabilities of the PCU are described in Section 3.5.

The PCU is capable of reporting to the DPC the status of any disk unit operating under its control in the event of an error condition associated with the unit. The PCU can also report the status of any disk unit upon command from the DPC. Particular error conditions detected by the PCU and the status reporting procedures followed by the PCU are discussed in Section 3.6.

The full set of disk command words accepted by the PCU from the DPC and the action taken by the PCU in response to each is given in Section 3.7. Section 3.8 discusses the basic IOC programming required to accomplish disk read, write and compare operations and supplies sample IOC instruction sequences for each of these operations.

3.2 Hardware Description

The PMSS is made up of 9 Singer Librascope L107MA-17-2100 disk memory units, which are fixed head-per-track type disk storage devices. Each disk unit provides a da'a storage capacity of

6.3×10^6 bits spaced over 100 tracks on the disk; has a maximum access time of 33 milliseconds; and operates at a transfer rate of from 1.8 to 2.3×10^6 bits per second.

The nine disk units provide a subsystem storage capacity of over 56×10^6 bits. Each of the nine units interfaces directly to an input/output channel on each of the PCUs. Two input/output channels are provided between a PCU and an IOA, via the EDU, for transferring data between the DPC and the Primary Mass Storage Subsystem. This configuration provides a PCU with the capability of controlling two disk units at the same time by dedicating each PCU/EDU/IOA channel to a particular disk unit. When both PCUs are being operated under load sharing, a total of four disk units could simultaneously be exchanging data with the DPC through the two PCUs. In the event that one PCU fails, the nine disk units can operate under the control of the other PCU which can select any two units at a time for data transfer.

Two disk units, which are also known as Primary Mass Storage Devices (PMSD), and the interface and power supply circuitry for each unit are normally contained in a single equipment enclosure called the Primary Memory Storage Unit (PMSU) (see Figures A.1 and A.2). The control switches for each disk unit are mounted on the front panel of the PMSU. The subsystem consists of 4 PMSUs with 2 disk units in each and 1 PMSU containing one disk unit. A block diagram of the PMSS is given in Figure 3.1.

The storage capacity of this subsystem can be expanded to satisfy growth requirements by the addition of nine more identical disk units and two more PCUs. These PCUs are the same as the units described earlier except in the area of input/output configuration. Each PCU will interface with an IOA, via the EDU, through the two 32 bit growth input/output channels of the IOA that are reserved for Primary Mass Storage expansion, and each unit will have nine input/output channels for interfacing with each of the added disk units. A tenth channel (growth) could be provided in each PCU similar to the tenth channel in the present FAH PCU. Thus, these PCUs through their design and programming will be dedicated to handling the added data transfer load resulting from the storage capabity expansion of this subsystem. The total storage capacity of the expanded subsystem will be in excess of 110×10^6 bits.

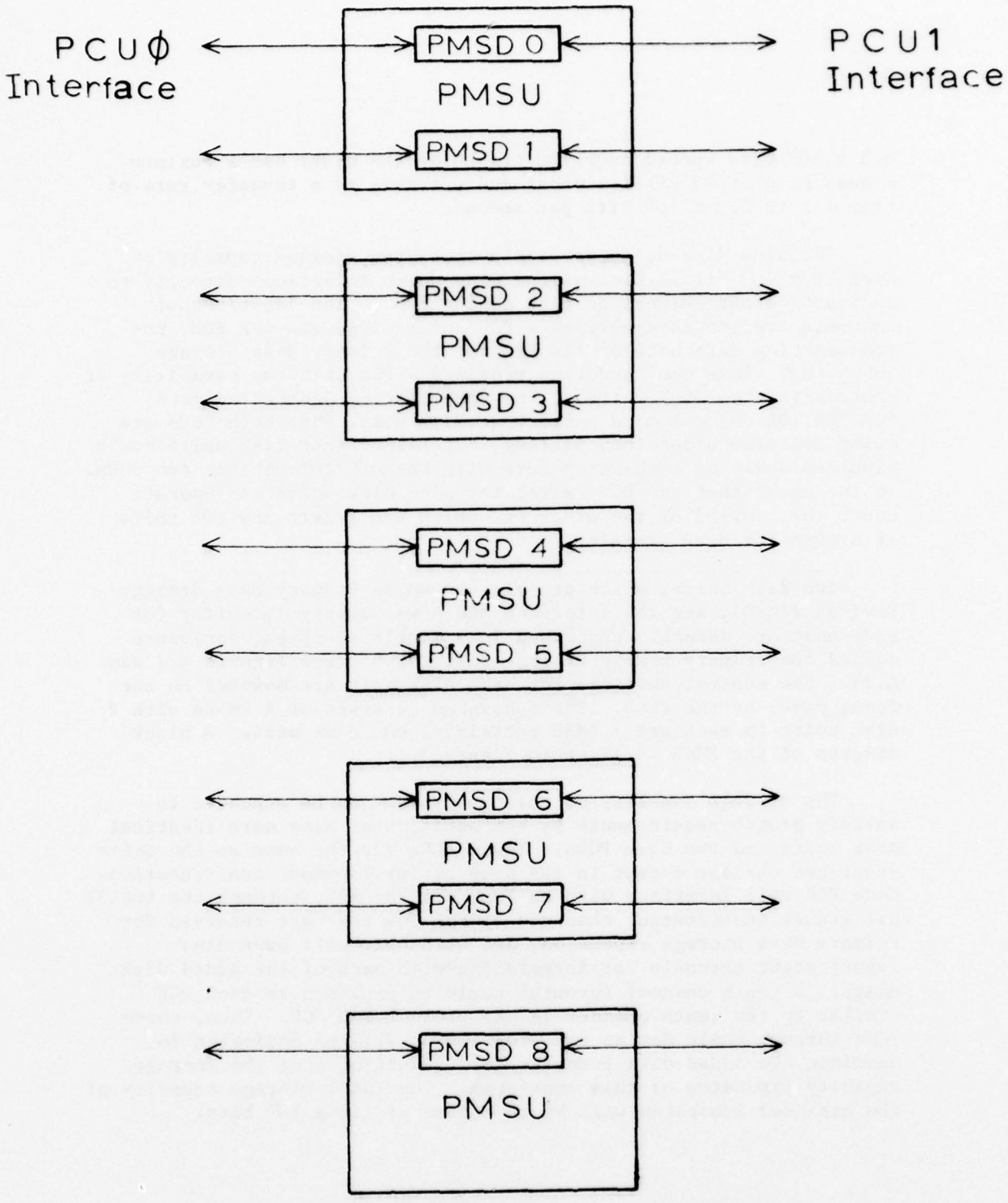
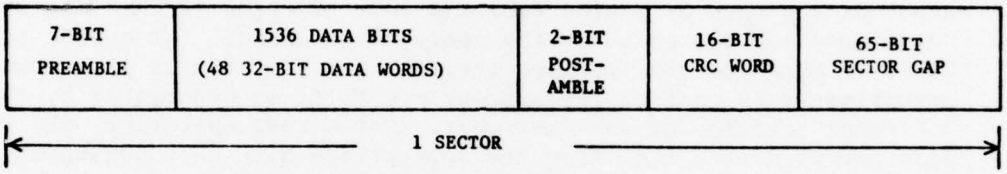


FIGURE 3.1. PRIMARY MASS STORAGE SUBSYSTEM BLOCK DIAGRAM

3.3 Data Formats

3.3.1 Disk Recording Format

Each disk unit is composed of 100 tracks with each track divided into 41 sectors. Each sector has the following format:



Each data transfer operation to or from a disk unit must read or write one or more full sectors of data (i.e., some multiple of 48 32-bit data words).

During each disk write operation, the PCU generates a Cyclic Redundancy Check (CRC) word for each sector as it is written and records it following the last data word of the sector. During each disk read operation, the PCU computes a CRC word for the sector as it is read and verifies the result with the CRC word recorded on disk for the sector.

3.4 Disk Functions

3.4.1 Data Transfer Functions

All disk data transfer functions are performed under the control of a PCU which, in turn, operates under the direction of commands received from the DPC. Operation of any of the nine disk units in the PMSS can be controlled by either of the DP&D's two PCUs, and data transfer between the DPC and the PCU can be performed on either of the two 32-bit PMSS channels of the PCU. The IOC associated with a PCU serves as the interface between the DPC and the PCU for the transfer of commands and data to the PCU and status information and data from the PCU.

Each disk read, write, or compare operation is initiated by the PCU in response to a control command received from the IOC via the external function capability of one of the PCU's two disk data transfer channels. The control command specifies the operation to

be performed, the disk unit to be used for the operation, and the track and sector on that unit at which the operation is to begin. The channel on which the command is sent to the PCU is the channel on which data words are transferred during the operation. During a write or compare operation, data words are transferred from the IOC to the PCU via the output data capability of a disk data transfer channel. During a read operation, data words are transferred from the PCU to the IOC via the input data capability of a disk data transfer channel. For a write operation, the PCU requests the output of one word at a time from the IOC. The IOC fetches one word from memory and places it on the appropriate channel for output to the PCU. When the PCU receives the data word, it writes it on the appropriate disk unit at the appropriate time, as determined by the rotational position of the disk unit. For a read operation, the PCU reads one word at a time from the appropriate disk unit beginning with the first word of the first sector to be used for the operation. It places the word on the appropriate channel and makes a request to the IOC for input of the data word. When the IOC receives the data word it stores it in memory. For a compare operation, the PCU reads one word at a time from the appropriate disk unit beginning with the first word of the first sector to be used for the operation. At the same time, the PCU requests the output of one word from the IOC. When the data word is received from the IOC, the PCU compares it with the corresponding data word read from disk. If the two words are not the same, the PCU detects the occurrence of a data compare error condition and provides an indication of the error as described in Section 3.6.

The number of words transferred during a disk operation and the main memory area to or from which they are transferred are controlled by the IOC and determined by an instruction in the IOC program directing the operation. When the IOC detects that the last data word has been transferred during a disk operation, it must issue a control command to the PCU to terminate the operation. The PCU, once it has initiated a disk operation, continues the operation until such a control command is received from the IOC.

3.5 PCU Disk Monitor Functions

In addition to controlling the transfer of data words to and from disk units, the PCU performs a number of monitor functions associated with disk operations. These functions are described in the following subsections.

3.5.1 Disk Selection/Deselection

Operation of any disk unit can be controlled by either of the DP&D's two PCUs. Disk selection/deselection is a programmable function which establishes which PCU is currently to control the operation of a given disk unit. A PCU can perform a data transfer operation to or from a particular disk unit only when that PCU is selected for control of that disk unit. Disk selection and deselection are implemented using the Load Disk Select Word Command discussed in Section 3.7. A PCU can be deselected for control of any disk unit at any time. A PCU can be selected for control of a given disk unit only when the other PCU has been deselected for control of that disk unit. Upon power-on or upon master reset of a PCU, the PCU is deselected for control of each of the nine disk units.

3.5.2 Read/Write Inhibit

Each PCU provides the capability to inhibit disk operations performed under its control. This inhibit capability is provided independently for reading and writing on a per track basis for each disk unit. Each PCU maintains four 32-bit read inhibit words and four 32-bit write inhibit words for each disk unit. The inhibit words in each PCU are numbered 0 through 35 for write inhibit and 0 through 35 for read inhibit, where write inhibit words 0-3 and read inhibit words 0-3 are for disk unit 0, write inhibit words 4-7 and read inhibit words 4-7 are for disk unit 1, etc.

Each disk track on a given disk unit is associated with one bit in the set read inhibit words for that disk unit and one bit in the set of write inhibit words for that disk unit. When the read inhibit bit in a given PCU for a given disk track is set to 0, that PCU is inhibited from reading data from that disk track; when this bit is set to 1, the PCU is enabled to read from the given disk track. The write inhibit bits control the inhibition of writing on disk tracks in a similar manner. The correspondence between bits in a set of four inhibit words (read or write) and tracks on a disk unit is as follows:

1st word:	bit:	31	30	29	28	.	.	.	0
	track:	0	1	2	3	.	.	.	31
2nd word:	bit:	31	30	29	28	.	.	.	0
	track:	32	33	34	35	.	.	.	63
3rd word:	bit:	31	30	29	28	.	.	.	0
	track:	64	65	66	67	.	.	.	95
4th word:	bit:	31	30	29	28	27	.	.	0
	track:	96	97	98	99	UNUSED			

Read and write inhibit words can be set and cleared by the DPC using the disk command words Load Upper Read Inhibit, Load Lower Read Inhibit, Load Upper Write Inhibit and Load Lower Write Inhibit. (See 3.7 for details). Upon power-on or upon master reset of a PCU, all bits of all inhibit words in the PCU are set to 0, (i.e., reading and writing is initially inhibited for all disk tracks).

3.5.3 Cyclic Redundancy Check

The PCU generates a 16-bit Cyclic Redundancy Check (CRC) word for each sector written to disk. The CRC word is written onto the disk unit following the last data word of the sector. When a disk sector is read during a read or compare operation, the CRC word for the sector is checked by the PCU to verify that the contents of the sector have not been altered since the sector was written. As the sector is read, the PCU recomputes a CRC word for the sector. After the last data word of the sector has been read, the PCU reads the CRC word recorded on disk for the sector and compares it with the CRC word computed during reading of the sector. If the two CRC words are not equal, the PCU provides an indication of a CRC error as described in Section 3.6.

3.5.4 Parity Generation and Check

All words transferred between the DPC and a PCU on the disk data transfer channels contain 32 data bits and one parity bit. The PCU generates odd parity on all data words and status words sent to the DPC and checks for odd parity on all data words and command words received from the DPC. If even parity is detected, the PCU provides an indication of a parity error as described in Section 3.6.

3.5.5 Data Timeout

The rate of rotation for each disk unit ranges from 27.0 revolutions per second to 33.3 revolutions per second. This rate of rotation requires a rate of data transfer between the DPC and the PCU within the range of one word (32 bits) every 13.8 microseconds to one word every 17.2 microseconds during disk read, write and compare operations. If the rate of data word transfer does not keep pace with the rate of disk rotation, the PCU senses that a data timeout error has occurred. The PCU provides an indication of the data timeout error in the manner described in Section 3.6.

3.6 Error Detection and Status Reporting

Each PCU maintains a 16-bit status word for each of the nine disk units in the Primary Mass Storage Subsystem. The status words residing in a given PCU are updated by the PCU to indicate error conditions associated with disk operations performed under the control of that PCU and to indicate other disk status information. Most error conditions associated with disk operations are reported to the IOC via the external interrupt capability of the disk channel used for the operation. In this event, the updated status word for the disk unit involved is transmitted as the external interrupt code word (see Appendix C). The status word for any disk unit is also transmitted to the IOC in response to a Read and Clear Status Word command. (See 3.7).

3.6.1 Error Conditions Detected

a. Command Word Conflict Error

A Command Word Conflict Error occurs when the PCU receives a disk control command which it cannot execute.

b. Read Inhibit Error

A Read Inhibit Error occurs when the PCU is commanded by the DPC to perform a read or compare operation involving a disk track for which the read inhibit bit is not set (i.e., reading is not enabled).

c. Write Inhibit Error

A Write Inhibit Error occurs when the PCU is commanded by the DPC to perform a write operation involving a disk

track for which the write inhibit bit is not set (i.e., writing is not enabled).

d. Data Timeout Error

During a disk read, write, or compare operation, a Data Timeout Error occurs when the rate of data transfer between the DPC and the PCU does not keep pace with the rate of rotation of the disk unit involved.

e. CRC Error

A CRC Error occurs when the CRC word generated for a disk sector during a read or compare operation does not equal the CRC word read from disk for that sector.

f. Data Compare Error

A Data Compare Error occurs when a data word read from memory during a compare operation does not equal the corresponding data word read from disk.

g. Data Parity Error

A Data Parity Error occurs when even parity is detected for a data word transferred to the PCU during a write operation or a compare operation.

3.6.2 Status Word Format

The status word for each disk unit includes an error indicator bit for each of the error conditions defined above. The disk status word format is as shown in Figure 3.2. Upon power-on or upon Master reset of the PCU, all error indicator bits (bits 15, 14, 13, 12, 9 and 8) in each of the PCU's nine disk status words are set to 0. When a PCU detects an error condition associated with a disk unit operating under its control, it sets the appropriate error indicator bit in its status word for that disk unit.

Additional status word bits are used to convey the following disk status information:

a. On-Line and Selected

When a PCU is selected for control of a given disk unit, bit 11 in the PCU's status word for that disk unit is set

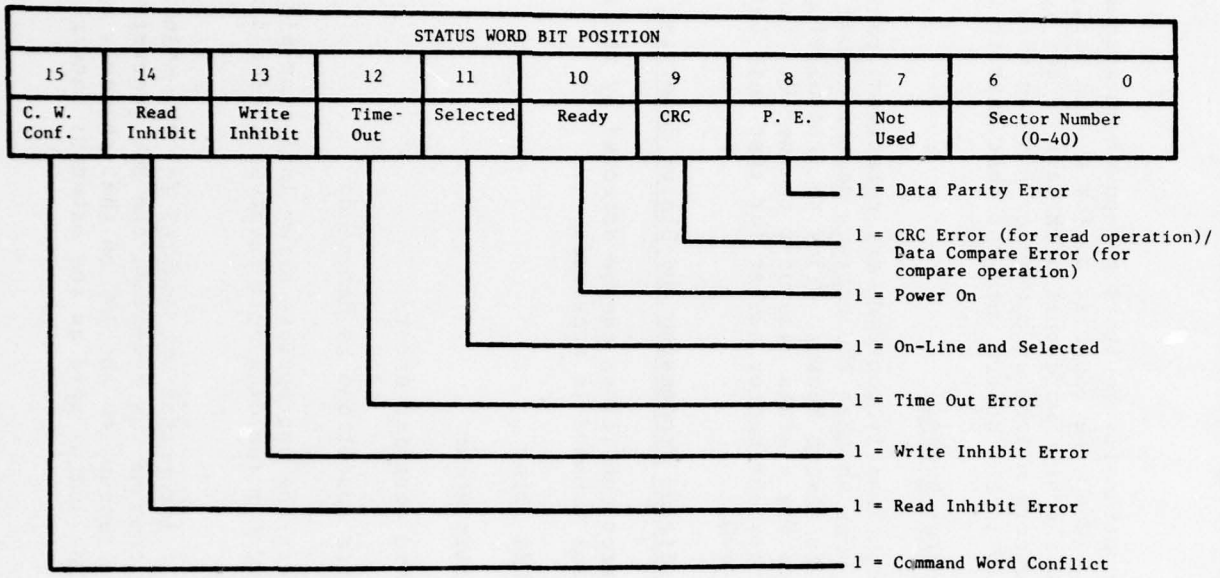


Figure 3.2. PCU Disk Status Word Format

to 1. When the PCU is deselected for control of the disk unit, this status word bit is set to 0.

b. Power-on

Each PCU continually monitors the power-on status of each disk unit. When the power is on for a disk unit, bit 10 in the PCU's status word that disk unit is set to 1. If the PCU detects a loss of power for a given disk unit, it sets bit 10 in the status word for that unit to 0.

c. Current Sector Number

Each PCU continually monitors the rotational position of each disk unit so that the current sector number for each disk unit is always known. Prior to transmitting the status word for a given disk unit to the IOC, the PCU loads the current sector number for that unit into status word bits 6-0.

3.6.3 Error Condition Processing and Status Reporting

The following error conditions can be detected by the PCU at the time a disk control command is received:

a. Read inhibit error

b. Write inhibit error

c. Command word conflict error

When one of these error conditions is detected:

a. the PCU sets the appropriate error indicator bit in the status word for the disk unit involved in the disk operation;

b. if external interrupts are enabled for the channel on which the command was received, the PCU generates an external interrupt to the IOC on that channel, using the updated disk status word as the external interrupt code word;

c. the PCU does not perform the function requested by the control command;

d. the PCU requests a new control command on the disk data transfer channel on which the error causing command was received.

A fourth error condition which can be detected by the PCU at the time a disk control command is received is a Command Word Parity Error. This error condition occurs when the PCU detects even parity for a word received via the external function capability of a disk data transfer channel. When such an error occurs, if external interrupts are enabled for the channel on which the word was received, the PCU generates an external interrupt on that channel using a fixed 16-bit external interrupt code word. This code word has bits 15 through 1 set to 1 and bit 0 set to 0. The function requested by the command is not performed, and the PCU makes a new request to the DPC for a command word on the channel over which the erroneous command was received.

The following error conditions can be detected by the PCU during a disk operation:

a. data parity error

b. CRC error

c. data compare error

d. data timeout error

When one of these error conditions is detected:

a. the PCU sets the appropriate error indicator bit in the status word for the disk unit involved in the disk operation;

b. the PCU continues the disk operation with which the error is associated;

c. if external interrupts are enabled for the channel on which data transfers for the operation are being performed, the PCU generates an external interrupt on that channel when the disk operation has completed (i.e., when a SRWO command has been received on that channel). The updated disk status word is used as the external interrupt code word. (NOTE: The sector number indicated in the updated disk status word is the number of the

sector at which the operation terminated, not the sector at which the error occurred.)

When a disk status word is transferred to the DPC as the result of an error condition, the error bits in the status word are not cleared by the PCU following the transfer. To clear the error bits in the status word for a particular disk unit, it is necessary for the DPC to issue to the PCU a Read and Clear Status Word (RCSW) command referencing that disk unit. (See 3.7).

3.6.4 Unreported Error Conditions

In addition to the error conditions described above, two error conditions can arise associated with disk operations which are not reported to the DPC.

a. Invalid Command Word

If a PCU receives a word via the external function capability of a disk data transfer channel which the PCU does not recognize as a valid disk command, the PCU attempts to execute the command. The result of an attempt to execute an invalid command word is unpredictable and is dependent upon the particular bit configuration of the command word. In general, no indication that an invalid command has been received by the PCU is given to the DPC. Following receipt of an invalid command word, the PCU must be master reset or powered off and then powered on again before successful operation of the PCU can be resumed.

b. Select Error

If a PCU is commanded by the DPC to perform a read, write, or compare operation for particular disk unit and the PCU is not selected for control of that disk unit, the PCU attempts to initiate the requested disk operation. The PCU, however, is inhibited from transferring any data to or from that disk unit, and, as a result, the requested disk operation is not performed. The PCU must be master reset before it can resume successful operation on the channel on which the inhibited disk operation was attempted.

3.7 Disk Control Commands

Disk control commands direct the PCU to perform control functions for the disk units. Disk control commands are provided to initiate and terminate disk operations and to establish selection and read/write inhibit control conditions. The format of each disk control command is given in Figure 3.3.

A description of the action taken by PCU in response to each command is outlined below. A disk control command is issued to the PCU by the IOC via the external function capability of a disk data transfer channel. A control command can be issued to a PCU, without force, on a particular channel only when the PCU requests receipt of a command via the external function capability of that channel. Upon power-on or upon master reset of a PCU, the PCU requests receipt of a control command on each of its disk data transfer channels. Following receipt of a control command on a given disk data transfer channel, the PCU will complete the function specified by the command before it requests receipt of another command on that channel. A control command can be issued to a PCU, with force, on a disk data transfer channel without waiting for a request from the PCU. Upon receiving a control command with force on a given channel, the PCU discontinues any function being performed associated with that channel and initiates the function specified by the new command. With the exception of the Stop Read Write Operation command (see below), disk control commands generally should not be sent to the PCU with force.

A. Read Disk Data Operation (RDDO)

a. From the information contained in the RDDO command, the PCU identifies the disk unit to be read from and the track and sector at which reading is to begin.

b. The PCU then examines the read inhibit bit for the specified track and disk unit.

c. If the read inhibit bit is set (i.e., reading is enabled), the PCU initiates a read operation from the specified disk unit.

B. Write Disk Data Operation (WDDO)

a. From the information contained in the WDDO command, the PCU identifies the disk unit to be written to and the track and sector at which writing is to begin.

COMMAND MNEMONIC	COMMAND WORD BIT POSITION																															
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RDDO	Disk No.* (0-9)				Unused					Track Number (0-99)							0	0	0	0	0	0	0	0	U	Sector Number (0-111)							
WDDO	Disk No.* (0-9)				Unused					Track Number (0-99)							0	0	0	0	0	0	0	1	U	Sector Number (0-111)							
WRCO	Disk No.* (0-9)				Unused					Track Number (0-99)							0	0	0	0	0	0	1	0	U	Sector Number (0-111)							
SRWO	Disk No.* (0-9)				Unused												0	0	0	0	0	0	1	1	Unused								
LURI	Inhibit Bits																0	0	0	0	0	1	0	0	U	Read Inhibit Word Number (0-39)							
LLRI	Inhibit Bits																0	0	0	0	0	1	0	1	U	Read Inhibit Word Number (0-39)							
LUWI	Inhibit Bits																0	0	0	0	0	1	1	0	U	Write Inhibit Word Number (0-39)							
LLWI	Inhibit Bits																0	0	0	0	0	1	1	1	U	Write Inhibit Word Number (0-39)							
RCSW	Disk No.* (0-9)				Unused												0	0	0	0	1	0	0	1	Unused								
LDSW	Unused				25 S* 9	S 8	S 7	S 6	S 5	S 4	S 3	S 2	S 1	S 0			0	0	0	0	1	0	1	0	Unused								

U - Unused S0-S9 = Select or deselect disks 0 through 9
ALL NUMBER VALUES ARE EXPRESSED IN DECIMAL

*The present DP&D system contains only 9 disk units (numbers 0-8).

Figure 3.3. Disk Control Command Formats

b. The PCU then examines the write inhibit bit for the specified track and disk unit.

c. If the write inhibit bit is set (i.e., writing is enabled), the PCU initiates a write operation on the specified disk unit.

C. Write Compare Operation (WRCO)

a. From the information contained in the WRCO command, the PCU identifies the disk unit to be used for comparison and the track and sector at which the comparison is to begin.

b. The PCU then examines the read inhibit bit for the specified track and disk unit.

c. If the read inhibit bit is set (i.e., reading is enabled), the PCU initiates a compare operation from the specified disk unit.

For each of the above commands, if the appropriate read or write inhibit bit is not set, the PCU does not initiate the requested operation. The PCU provides an indication of a read or write inhibit error as described in Section 3.6.

D. Stop Read/Write Operation (SRWO)

The PCU stops the read, write, or compare operation currently being performed on the channel over which the SRWO command was received.

E. Load Upper Read Inhibit Word (LURI)

The PCU loads the 16 bits of read inhibit data contained in the LURI command word into the most significant half (bits 31-16) of the specified read inhibit word.

F. Load Lower Read Inhibit Word (LLRI)

The PCU loads the 16 bits of read inhibit data contained in the LLRI command word into the least significant half (bits 15-0) of the specified read inhibit word.

G. Load Upper Write Inhibit Word (LUWI)

The PCU loads the 16 bits of write inhibit data contained in the LUWI command word into the most significant half (bits 31-16) of the specified write inhibit word.

H. Load Lower Write Inhibit Word (LLWI)

The PCU loads the 16 bits of write inhibit data contained in the LLWI command word into the least significant half (bits 15-0) of the specified write inhibit word.

I. Read and Clear Disk Status Word (RCSW)

a. If external interrupts are enabled* for the channel on which the RCSW command was received, the PCU generates an external interrupt to the IOC on that channel using the disk status word for the disk unit specified by the RCSW command as the external interrupt code word. If external interrupts are not enabled, no external interrupt is generated.

b. The PCU then clears the error bits (15-12, 9-8) in the disk status word for the specified disk unit. These error bits are cleared regardless of whether the status word is transmitted to the IOC. If the status word is transmitted, the error bits are cleared after transmission.

---

* External interrupts are enabled for a given channel on a given IOC as a result of the execution by that IOC of a particular IOC instruction referencing that channel. This is discussed in detail in Section 3.8.

J. Load Disk Select Word (LDSW)

a. The PCU issues a selection request to each disk unit for which the corresponding bit in the LDSW command word is set to 1.

b. The PCU issues a deselection request to each disk unit for which the corresponding bit in the LDSW command word is set to 0.

c. Deselection requests will always be honored. Following a deselection request, the requesting PCU is deselected for control of the disk unit to which the request was made. Selection requests issued by one PCU will be honored only when the other PCU is not currently selected for control of the disk unit to which the request was made. If a selection request is honored, the requesting PCU is selected for control of the disk unit to which the request was made. If a selection request issued by PCU X is not honored, it remains pending until a) PCU X issues a deselection request to that disk unit or b) PCU Y issues a deselection request to that disk unit. In the latter case PCU X becomes selected for control of the disk unit. Each PCU maintains a status word for each of the nine units. One bit in the status word for each disk unit is used to indicate the select status of the PCU with respect to that disk unit. When the PCU is selected for control of a disk unit, the select bit in the status word for this disk unit is set to one. When the PCU is deselected this bit is set to 0.

Following execution of an SRWO, LURI, LLRI, LUWI, LLWI, RCSW, or LDSW command, the PCU requests receipt of another command from the IOC on the disk data transfer on which the initial command was received. Following receipt of an RDDO, WDDO, or WRCO command on a given disk channel, the PCU does not request receipt of another command on the given channel until an SRWO command is received on that channel to terminate the disk operation initiated by the RDDO, WDDO, or WRCO command. The SRWO command must therefore be sent to the PCU with force. All other disk control commands should be sent to the PCU without force.

3.8 Programming for Disk Operations

The previous sections of this discussion of the PMSS have concentrated on the role of the PCU as a controller for disk

operations and the disk control commands which direct the operation of the PCU. Performance of any disk operation requires the transfer of a sequence of control commands and data words between memory and the PCU. These transfers are initiated and controlled by the IOC as it executes a chain of IOC instructions stored in memory. The CPU can direct an IOC to execute a particular chain of IOC instructions by executing an Initiate I/O instruction which references that IOC and specifies the memory address of the first IOC instruction in the chain.

This section discusses the construction of chains of IOC instructions which initiate the appropriate sequences of command and data word transfers to accomplish basic disk operations. A review of the individual IOC instructions which initiate transfers between memory and peripheral devices is provided in Appendix C.

All examples in this section use the coding conventions of AN/UYK-7 Assembler (DPDASM) documented in Reference 3. All numbers used are represented in decimal unless the first digit of the number is a 0. In this case, the number is represented in octal. The letters j, y, k, c, m are used to identify the operands of an IOC instruction as described in Appendix C.

3.8.1 Preparations for Read, Write, or Compare Operations

3.8.1.1 External Interrupt Enabling. Error conditions associated with a disk operation may be detected by the PCU either upon receiving a command requesting initiation of the operation (e.g., write inhibit violation, command word parity error) or during the transfer of data words for the operation (e.g., data parity error, data timeout error). If a report of any error condition which may arise associated with a disk operation is desired, external interrupts should be enabled on the channel to be used for the operation prior to initiation of the operation. (Moreover, a command word parity error may occur whenever any command word is sent to the PCU. To ensure that the DPC is notified of all command word parity errors, external interrupts should generally be enabled on a disk data transfer channel before any command words are sent to the PCU on that channel.)

Example:

Execution of the following IOC instruction chain enables an external interrupt to occur on channel 12 of the IOC executing the chain:

```
                    j       y       k     c     m
EIEN        XB     12,    EIBCW,    3,    0,    1

EIBCW       BCW  EIBUF, 1        . Buffer Control Word

EIBUF       RES    1             . one-word status word buffer
```

The XB (Initiate External Interrupt Buffer) instruction permits an external interrupt to occur on channel 12 and initiates a one-word buffer in main memory for input of a disk status word in the event of an external interrupt. The buffer control word at address EIBCW specifies that the disk status word transmitted as the external interrupt code word will be loaded into the one-word buffer at main memory address EIBUF. The k-field specifies that the 16-bit status word will be loaded into bits 15-0 of location EIBUF. The c-field specifies that the XB instruction is the last instruction in the chain. The m-field specifies that a class 3 monitor interrupt is to be generated to the CPU in the event of an external interrupt on channel 12.

3.8.1.2 Establishing Selection and Inhibit Control Conditions. Prior to initiating any disk operation the following preliminary tasks must be performed:

a. A PCU must be selected for control of the disk unit to be used in the operation.

b. The appropriate inhibit bit must be set to enable reading or writing of the disk track to be used in the operation.

These two tasks can be accomplished by sending a Load Disk Select Word (LSDW) command and a load inhibit word command (LURI, LLRI, LUWI, LLWI) to the PCU which is to control the disk operation. It is recommended that following the transfer of these commands to the PCU, the status word for the disk unit to be used be read (via an RCSW command to the PCU) and examined to verify that selection was successful.

Example:

Execution of the following IOC instruction chain by a given IOC instructs the PCU associated with that IOC to request to be selected for control of disk unit 6 and sets the appropriate inhibit bit in that PCU to enable writing on track 1 of disk unit 6.

```
                j     y      k     c     m
INIT    FB     12,  LDSW,   1,    1,    0
        FB     12,  LUWI,   1,    0,    1
LUWI  +010000003030    .Load Upper Write Inhibit command
LDSW  +020005000       .Load Disk Select Word command
```

Each of the FB instructions in this chain issues one command word to the PCU on channel 12. These commands are issued without force (k=1), and a monitor interrupt is requested with the transfer of the second command word. The first FB instruction issues a Load Disk Select Word command directing the PCU to issue a selection request to disk Unit 6 (and a deselection request to all other disk units). The second FB instruction issues a Load Upper Write Inhibit command directing the PCU to enable writing for track 1 of disk unit 6.

3.8.2 Read, Write, and Compare Operations

When the preliminary tasks described above have been accomplished, the desired disk operation can be performed. A simple disk operation can be accomplished with a single IOC instruction chain of the following general form:

FB (without force) to issue a disk control command (WDDO, RDDO or WRCO) to the PCU to initiate the operation.

IB (or OB) to initiate the transfer of data words to (or from) memory.

FB (with force) to issue a disk control command (SRWO) to the PCU to stop the operation.

The first FB instruction directs the IOC to initiate the output of one word as a command to the PCU. This command is sent to the PCU on the disk data transfer channel referenced by the FB instruction and it is sent without force. A Write Disk Data Operation (WDDO) command is sent to initiate a write operation, a Read Disk Data Operation (RDDO) command to initiate a read operation, and a Write Compare Operation (WRCO) command to initiate a compare operation. From the information contained in this command word, the PCU identifies the disk unit to be used for the operation and the track and sector at which the operation is to begin. The

PCU then initiates the requested disk operation. The channel on which the command word was received by the PCU is the channel on which the PCU requests or sends data words to the IOC during the operation. The PCU continues the disk operation until it receives a subsequent command word on this same channel directing it to stop the operation.

An OB instruction directs the IOC to initiate the output of data words from memory to the PCU on the disk data transfer channel referenced by the OB instruction. The buffer control word referenced by the OB instruction defines the number of words to be output and the location of the main memory buffer from which they are to be output. An IB instruction directs the IOC to initiate the input of data words from the PCU on the disk data transfer channel referenced by the IB instruction. The buffer control word referenced by the IB instruction defines the number of words to be input and the location of the main memory buffer to which they are to be input. The OB or IB instruction must reference the same channel referenced by the initial FB instruction.

During the input/output operation, the IOC keeps track of the number of words to be transferred (as specified by the buffer control word referenced by the IB or OB instruction). When transfer of the last data word has been completed, the IOC executes the final FB instruction. This instruction directs the IOC to transfer a Stop Read Write Operation (SRWO) command to PCU. This command must be sent to the PCU with force and must be sent on the same channel used for the data transfer operation. This command directs the PCU to terminate the disk operation. If a SRWO command is not issued to the PCU, the PCU will continue to request the IOC to send or accept data words for this operation. The IOC will not honor these requests, and a data timeout error will result.

Example: Read Operation

Execution of the following IOC chain by a given IOC will result in the transfer of one block of 96 32-bit words from track 50, sectors 10-11, of disk unit 1 to the main memory buffer beginning at location RDBUF. Data transfers will be performed on channel 14 of the given IOC and one EF (external function) monitor interrupt is generated upon completion of the last IOC instruction in the chain.

```
                    j       y       k       c       m
READ        FB      14,     RDDO,   1,      1,      0
            IB      14,     RDBCW,  3,      1,      0
            FB      14,     SRWO,   0,      0,      1
RDDO    +02014400012
SRWO    +02000001400
RDBCW   BCW   RDBUF,96  . Buffer control word for input buffer
RDBUF   RES   96        . 96-word input buffer
```

Example: Write Operation

Execution of the following IOC instruction chain by a given IOC will result in the transfer of one block of 1968 32-bit words from the main memory buffer starting at location WRTBUF to track 5 (sectors 0-40) of disk unit 2. Data transfers will be performed on channel 12 of the given IOC and one EF monitor interrupt is generated upon completion of the last IOC instruction in the chain.

```
                    j     y       k     c     m
WRITE       FB    12,  WDDO,     1,    1,    0
            OB    12,  WRTBCW,   3,    1,    0
            FB    12,  SRWO,     0,    0,    1

WDDO        +04001200400        . Write Disk Data Operation command
SRWO        +04000001400        . Stop Read/Write Operation command
WRTBCW      BCW WRTBUF, 1968    . Buffer Control Word for output
                                  buffer
WRTBUF      RES 1968            . 1968-word Output buffer
```

Example: Compare Operation

Execution of the following IOC instruction chain by a given IOC will result in the comparison (by the PCU associated with the given IOC) of a block of 480 32-bit words read from track 1, sectors 0-9, of disk unit 9 with a block of 480 32-bit words transferred to the PCU from the main memory buffer beginning at location CMPBUF. Data will be transferred to the PCU on channel 12. One EF monitor interrupt will be generated upon completion of the last IOC instruction in the chain.

```
                    j       y       k       c       m
COMPARE     FB      12,     WRCO,   1,      1,      0
            OB      12,     CMPBCW, 3,      1,      0
            FB      12,     SRWO,   0,      0,      1
WRCO        +022000201000       . Write Compare Operation command
SRWO        +022000001400       . Stop Read/Write Operation command
CMPBCW      BCW CMPBUF,480      , Buffer Control Word for output
                                  buffer
CMPBUF          RES 480         . Output buffer
```

4.0 THE SECONDARY MASS STORAGE SUBSYSTEM (SMSS)

4.1 Introduction

This section treats the SMSS of the DP&D Subsystem in a manner similar to that given the PMSS in Section 3.0. Here we are primarily concerned with the actions required for a programmer to:

1. WRITE on the magnetic tape numbered N a block of words stored in the main memory.

2. READ a block of words from the magnetic tape numbered N for the purpose of transferring same to main memory.

The essence of this section is to be found in subsection 4.8, wherein illustrative examples of WRITE and READ operations are presented in considerable detail. The examples are simplistic in that they stand alone and do not reference any other portion of a larger program as would most likely be the case in a real programming endeavour. While elementary, the examples are pedagorically sound in the sense that they demonstrate how one might effect the transfer of a specified block of data from main memory to a specified tape (or vice versa), allow for error interrupts, keep track of the status of the hardware involved in the transfer, and stop the tape. The value of the examples lies in the fact that the programmer is made aware of information that must be supplied to the system as well as conventions that apply to the system. This approach is consistent with the policy stated in the Introduction wherein it was declared that no attempt would be made to suggest programming discipline.

4.2 Hardware Description

The secondary mass storage subsystem is made up of four UNIVAC type 1840 Magnetic Tape Transport Units (MTTU) and four Dual Interface Operator Units (DIOU) that are built by General Dynamics.

The DIOU is used to provide the data transfer interface between an MTTU and two Peripheral Control Units (PCUs). Each MTTU, which is also known as an RD-366/USH-20(V) Magnetic Tape Transport, interfaces directly to a DIOU, and each DIOU interfaces directly to an input/output channel on each PCU. The DIOU contains the control switches and indicators for the MTTU, including a unit select identification switch. A block diagram of the SMSS is given in Figure 4.1.

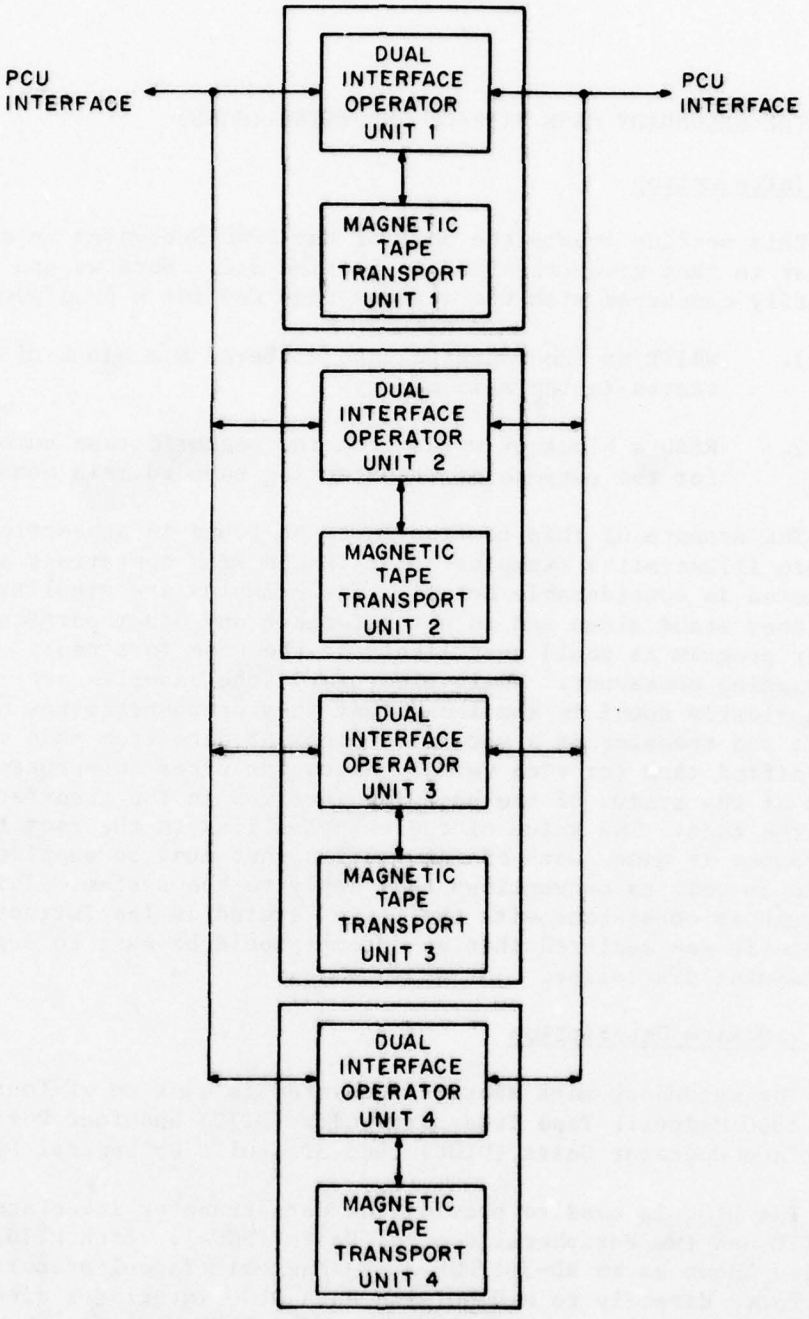


Figure 4.1 SECONDARY MASS STORAGE SUBSYSTEM BLOCK DIAGRAM

Each MTTU records data on 1/2 inch, 9 track magnetic tape at a tape speed of 75 inches per second with a recording density of 800 bits per inch. Each MTTU uses magnetic tape, tape reels, markers, format, and recording features that comply with American National Standard X3.22-1967.

The DIOU, in addition to allowing for PCU control of the MTTU, provides for manual control of same. The functional distinction between manual and computer control is as shown in Figure 4.2. In that this working paper is concerned with computer programming, the manual aspects of the DIOU shall warrant no additional comments.

Two input/output channels are provided between a PCU and an Input/Output Adapter (IOA), via the Error Detection Unit (EDU), for transferring data between the computer subsystem and the secondary mass storage subsystem. This configuration provides a PCU with the capability of controlling two MTTUs at the same time by dedicating each PCU/EDU/IOA channel to a particular MTTU (see Section 4.4.3 for more on this point).

4.3 Data Formats

4.3.1 Tape Recording Formats

The MTTU recording formats are in full compliance with USAS X3.22-1967 with the exception that the Block Length restrictions of 6.5 are not observed. The MTTU interface control signals are implemented and controlled by the PCU to support the format detailed in USAS X3.22-1976.

The 9-Track Tape Format for a recording density of 800 frames-per-inch (fpi) is as given in Figure 4.3.

In discussing the actual placement of data and a magnetic tape one frequently encounters the words "record", "file", and "tape mark". Graphic representations of these terms are afforded by Figure 4.4 and elaborated upon below.

4.3.1.1 Record. Data is recorded on magnetic tape in variable length records under program control with odd lateral and logitudinal parity added and checked by the PCU. Record size for the 9-track 800-frame-per-inch density must contain at least 18 USASCII characters (one 16-bit word plus two parity bits) with the upper bound being the entire storage capacity of a tape.

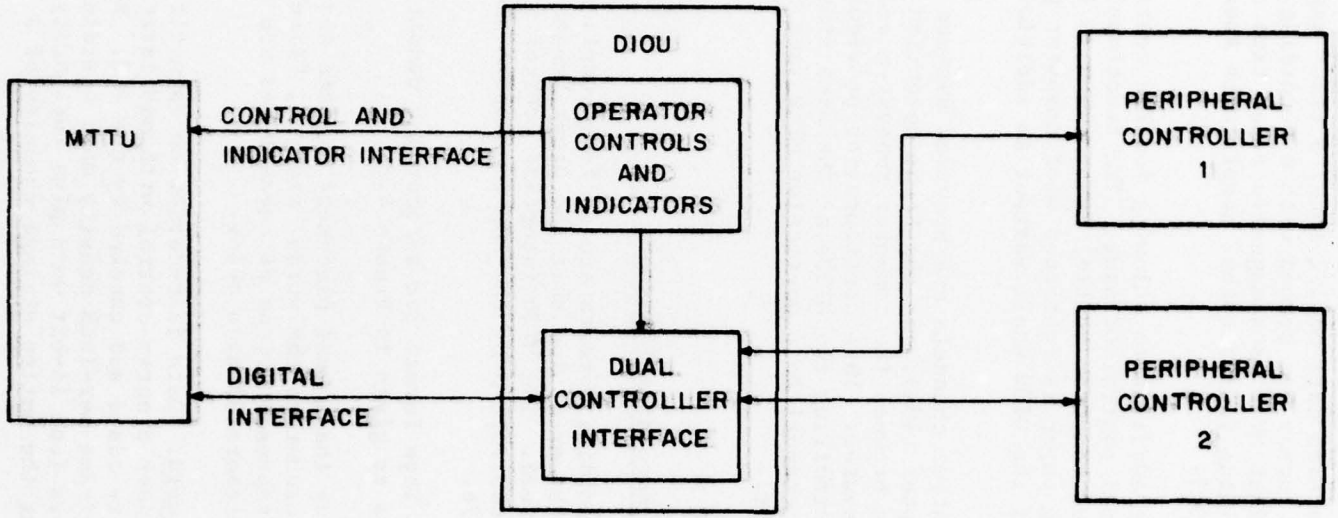


Figure 4.2 DIOU BLOCK DIAGRAM

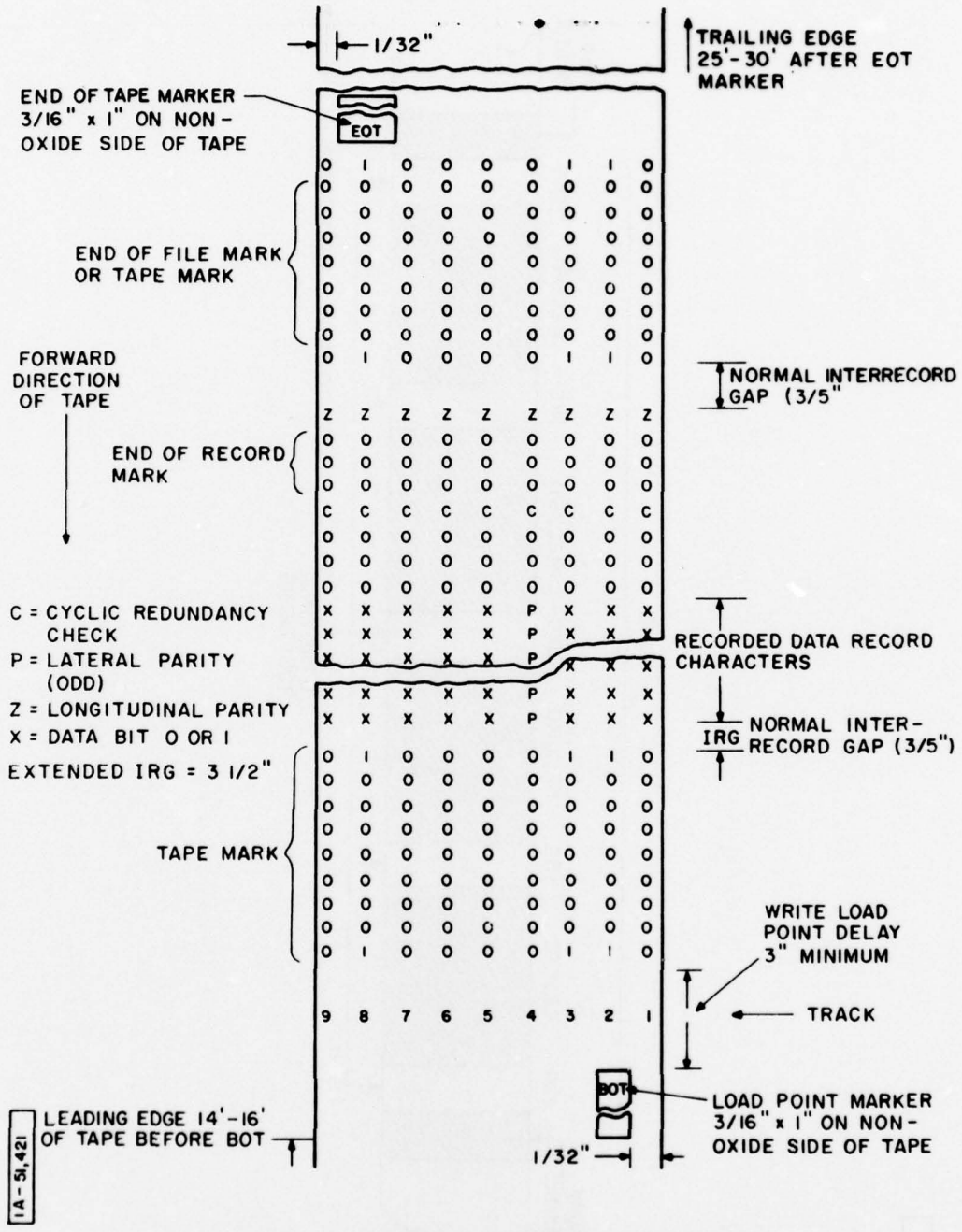


Figure 4.3 9-TRACK TAPE FORMAT (800 fpi)

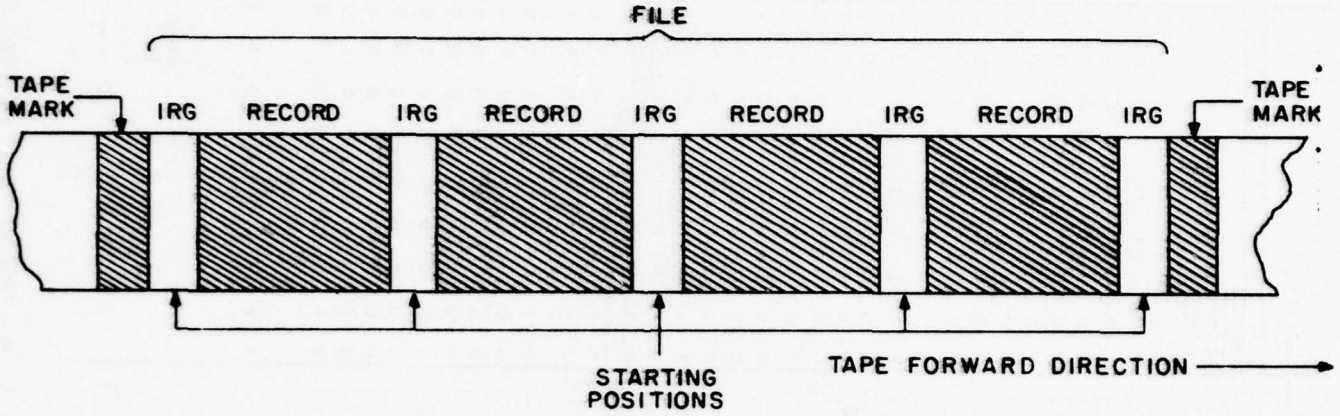


Figure 4.4 RECORD/FILE FORMAT

4.3.1.2 File. A file consist of one or more records, each record being separated by an interrecord gap (IRG). End of file is followed by an IRG and a tape mark.

4.3.1.3 Tape Mark (File Mark). The structure of the tape mark for the 9-track (800 fpi) tape is as shown in Figure 4.3.

A tape mark can be written as the first frame on the tape after the BOT marker, as shown. However, this is a programmer's option, not a requirement; the first frame may consist of data received from memory.

For additional information concerning tape format, the reader is referred to Reference 4, pp. 4-7 to 4-13.

4.3.2 Data Transfer Format

Tape data is transferred between the PCU and the Data Processor in the form of 16-bit words via a 16-bit channel. Each data word contains two 8-bit characters with the upper half (bits 8 through 15) of the data word preceding the lower half (bits 0 through 7) for transfer between the MTTU and the PCU. For the Read Record Frame Mode (see Section 4.7), 9-bit characters are transferred including the character parity, cyclic redundance check (CRC) and longitudinal check (LRC) check data as read from the tape, with one character packed in each 16-bit word, in bits 0 through 8 with the parity bit in bit position 8. The format for the lower half word is identical to that for a normal data transfer and the upper half word contains zeroes except for bit 8.

4.4 Tape Functions

4.4.1 Data Transfer Functions

4.4.1.1 Write Data. The PCU directs the writing of data blocks on magnetic tape on each MTTU. Eight-bit data characters plus parity are recorded on nine parallel tracks. The timing of the write strobe generated by the PCU yields a tape data density of 800 characters per inch with a tape speed of 75 inches per second. Provisions are made for an initial gap between BOT and the first data record on the tape reel of 3 inches, and for gaps between subsequent records of 0.6 inch. When a write command is initiated with the tape at the BOT marker, the PCU calls for an additional delay causing a minimum 3 inch of tape travel before the first data character is recorded. Records have a length ranging from 18 USASCII characters to the entire storage capacity of a tape.

The PCU reformats the data words received from the Data Processor, computes the parity bit to be recorded with each 8-bit character, and continuously computes the CRC for each complete record. The CRC is formatted in the fourth character position following the final data character, and the LRC in the eighth. Recording of the LRC is controlled by the coincidence of the write reset signal with the write strobe. This coincidence of interface signals results in the LRC character being recorded by the MTTU.

Capability is included in the PCU to format and transfer data to the MTTU so as to record the tape mark which is a single character record as described in USAS X3.22-1967.

During each write operation, a read is performed as the previously recorded data passes under the read head. Error checking procedures including character parity checking, CRC generation and checking and LRC checking are performed at this time.

4.4.1.2 Read Data. The PCU controls reading of a complete record beginning with the first data characters encountered after the start of the magnetic tape motion. Provisions are made to accommodate an initial 3 inch gap between BOT and the first data character on the tape reel; and for subsequent gaps between records of 0.6 inch. The 8-bit data characters are assembled into 16-bit data words and transferred to the Data Processor. Read control is accomplished via the read enable and read strobe interface signals. Parity is checked for each 8-bit character and the CRC and LRC characters are continuously generated as a function of each character read throughout each complete record and compared to the CRC and LRC characters read at the completion of a complete record. If an error is detected, the PCU does the following:

a. Sets the error detected bit in the applicable Tape Status Word.

b. Issues an external interrupt using the applicable status word as the interrupt code.

The CPU recognizes tape marks as the tape is transported in either the forward or reverse directions in order to support the count tape mark functions (see 4.4.2.2).

4.4.1.3 Search Key Word. Searching for a record based on the first character (eight bit) of the record is employed for record identification. As the tape is transported forward, the first character of each record is read and compared to the "Key Word"

character (eight bits) contained in the command word. When equality is found, the tape is advanced to the end of the block, direction of tape travel is reversed, and the tape is stopped in the IBG prior to the desired eight bits. The search is conducted from the starting point until detection of a tape mark, where it stops should the search criteria be not satisfied.

4.4.2 Non-Data Transfer Functions

4.4.2.1 Count Interblock Gaps. The PCU is designed to count a specified number of IBGs as the tape is transported forward or backward, and to stop the tape in the gap at the end of the count. IBGs are identified by the absence of tape data for more than eight tape character times. The forward motion terminates upon detection of a tape mark. The reverse motion terminates upon detection of a tape mark or BOT.

4.4.2.2 Count Tape Mark. The PCU is designed to count a specified number of tape marks as the tape is transported forward or backward, and to stop the tape in the IBG following the tape mark at the end of the count. Identification of the tape mark involves recognition of the DC3 character (reference USAS X3.22-1967, paragraph 6.5.1) immediately following an IBG, followed by 7 all zero characters (the CRC character is all zeroes) and another DC3 character. The forward motion terminates upon detection of a tape mark. The reverse motion terminates on BOT.

4.4.2.3 Rewind. The rewind function is initiated by the PCU. When the BOT indication is received, BOT status information is stored by the PCU in the appropriate tape status word.

4.4.3 Simultaneous Function Capability

The PCU has the capability to support data transfer functions on two MTTUs simultaneously with non-data transfer functions on the remaining MTTUs. Data transfer functions include Write Data, Read Data, and Search Key Word. Non-data transfer functions include Rewind, Count Interblock Gaps, and Count Tape Marks where the counter number equals one. When both PCUs are being operated under load sharing, all four MTTUs can simultaneously exchange data with the computer subsystem through the two PCUs.

Normally, each PCU multiplexes its two EDU/IOA secondary mass storage channels with its four tape transport channels in order to provide each PCU with the capability of controlling the complete subsystem in the event that one PCU fails.

4.5 PCU Tape Monitor Functions

In addition to controlling the transfer of data words to and from tape units, the PCU performs a number of monitor functions associated with tape operations. These functions are described in the following sections.

4.5.1 Tape Selection/Deselection

The Select Request signal received from the PCU informs the DIOU that a PCU is requesting to be selected for MTTU control. The DIOU uses the Select Request signals and the peripheral controller selection switch logic to establish which controller is to be selected. The DIOU selects the peripheral controller in accordance with the following:

a. Peripheral Controller 1: Peripheral Controller 1 is selected when its Select Request signal is a logical one and the following conditions are met:

   (1) Peripheral controller selection switch, Controller 1, is in the AUTO position.

   (2) Peripheral Controller 2 Select Request is a logical zero.

b. Peripheral Controller 2: Peripheral Controller 2 is selected when its Select Request signal is a logical one and the following conditions are met:

   (1) Peripheral Controller selection switch, Controller 2, is in the AUTO position.

   (2) Peripheral Controller 1 Select Request is a logical zero.

Once the DIOU has selected either Peripheral Controller 1 or 2, the DIOU shall retain selection of that peripheral controller so long as the selected peripheral controller Select Request signal remains a logical one and the selected peripheral controller selection switch is not placed in the DISABLE position. Under no condition does the DIOU allow both peripheral controllers to be selected at the same time. When a PCU is "deselected" for control of a tape unit, data transfers to and from that tape unit cannot be performed on the tape channels of that PCU. A PCU can be deselected for control of any tape unit at any time. A PCU can be selected for control of a given

tape unit only when the other PCU has been deselected for control of that tape unit. Upon power-on or upon master reset of a PCU, the PCU is deselected for control of each of the four tape units.

4.5.2 Cyclic Redundancy Check/Longitudinal Redundancy Check

The PCU generates a 9-bit Cyclic Redundancy Check (CRC) word at the end of each tape record. CRC is transferred to the MTTU at the end of each data record. The details associated with the computation of CRC are given in Section 4.6.1.1.

In addition to computing CRC, the PCU generates an additional check for data transfers involving a tape unit. Following the CRC, a Longitudinal Redundancy Check (LRC) is written for the possible detection of read errors (see Section 4.6.1.2).

4.5.3 Parity Generation and Checking

All words transferred between the PCU on the tape data transfer channels contain 16 data bits and one parity bit. The PCU generates odd parity on all data words and status words sent to the IOC and checks for odd parity on all data words and command words received from the IOC. If even parity is detected, the PCU provides an indication of a parity error as described in Section 4.6.

4.5.4 Data Transfer Timeout

During a read or write operation the tape moves at a speed of 75 inches per second. A tape density of 800 characters per inch is translated into 60,000 characters per second. Should the rate of data word transfer not keep pace with the rate of tape rotation, the PCU senses that a data timeout error has occurred. The PCU provides an indication of the data timeout error in the manner described in Section 4.6.1.3.

4.6 Error Detection and Status Reporting

Two ever present concerns of the programmer are the detection of errors and the status of the hardware under software control. An important distinction exists between the PMSS and the SMSS in that at the completion of all tape commands, the PCU transmits a 'task completed' status word (see 4.6.3.2 below).

4.6.1 Error Detection

External interrupt code words are transmitted when certain errors are detected by the PCU. The exact error condition and resultant code word are defined later in this section along with the specified error detection capability. When a specified error detection requires a resultant external interrupt and the external interrupt enable line is not set, the external interrupt is inhibited.

4.6.1.1 The Cyclic Redundancy Check. At the end of each tape block, a character is written on the tape for the possible recovery of single-track errors. This character is called the Cyclic Redundancy Check (CRC) character. In tape mark blocks, zero bits are written in all tracks for the CRC character.

Consider the contents of a 9-position register to be C1 to C9 with the following track assignments:

Regular position: C1 C2 C3 C4 C5 C6 C7 C8 C9

Track number: 4 7 6 5 3 9 1 8 2

The CRC character is derived as follows:

A. All data characters in the tape block are added to the CRC register without carry (each bit position is exclusive OR'ed to Cn).

B. Between additions, the CRC register is shifted one position C1 to C2, etc., and C9 to C1.

C. If shifting will cause C1 to become "1", then the bits being shifted into positions C4, C5, C6, and C7 are inverted.

D. After the last data character has been added, the CRC register is shifted once more in accordance with B and C above.

E. To write the CRC character on tape, the contents of all positions except C4 and C6 are inverted. The parity of the CRC character will be odd, if the number of data characters within the block is even, and even, if the number of data characters within the block is odd. The

CRC character may contain all-zero bits in which case the number of data characters was odd.

4.6.1.2 The Longitudinal Redundancy Check. Following the CRC character, a check character is written for the possible detection of read errors. This character is called the Longitudinal Redundancy Check (LRC) character. A longitudinal check bit is written in any track if the longitudinal count is otherwise odd.

4.6.1.3 Data Transfer Time-Out. A data transfer time-out capability is provided. If the Data Processor channel does not support the necessary data transfer rates required to accomplish a proper data write or data read function, the PCU issues a tape data time-out indication. If a data time-out indication occurs, the PCU performs the following:

A. Sets the time-out PCU indication bit in the appropriate tape status word.

B. Issues an external interrupt using the appropriate tape status word as the external interrupt code word.

4.6.1.4 Parity Errors. During a write operation, the PCU receives 16-bit data words from the AN/UYK-7 which it reformats into two 8-bit characters for transfer to a tape. Parity is computed for each 8-bit character. As the data passes under the read head in the MTTU, character parity checking occurs. Any single character parity error is detected at this time. During a read operation, the parity is again checked for each 8-bit character as it is read off the tape.

The response to the detection of a parity error is given below (4.6.3.3).

4.6.1.5 Command Word Conflict. When a command word is such that its execution would violate a system constraint, the command word conflict bit is set in the PCU tape status word. The illegal operation might be, for example, a request to access a busy tape unit or a request that exceeds the simultaneous access capability.

4.6.2 Tape Status Word Format

Tape status words are used to convey status information relative to each of the MTTUs to the Data Processor. Each PCU contains a tape status word for each of the four MTTUs. All MTTU command words which require a direct response from a MTTU result in

the storage of status information in the PCU. MTTU identification is provided in each tape status word. This identification includes the absolute address of the MTTU, and the state of the two Unit Identification signals (UI0 and UI1) selectable via the Unit Select switches associated with each MTTU. The two absolute MTTU address bits (TA0 and TA1) are determined by the PCU connector to which a MTTU is connected. The status word format is as shown in Table IV-1. Upon power-on or upon master reset of a PCU, the error indicator bits (bits 6, 9, 12, and 13) in each tape status word in that PCU are set to 0.

4.6.3 Status Reporting

The details associated with reporting the status of a given tape unit, for three different circumstances, are presented in this section.

4.6.3.1 Read Tape Status Word. The PCU will report the status of any tape unit in response to a Read Tape Status Word (RTSW) command referencing that tape unit. Upon receiving such a command, the PCU will transmit the specified tape status word to the IOC via the external interrupt capability of the tape channel on which the RTSW command was received. The PCU will then set all error bits (bits 6, 9, 12, and 13) to 0 in the status word transferred. As is always the case, the transfer of status in response to an RTSW command will occur only if external interrupts are enabled on the tape channel to be used. Error bits in the specified status word will be cleared regardless of whether the status word transfer occurs.

4.6.3.2 Tape Task Completion. The external interrupt capability is used to signify completion of a tape command function. Upon completion of a task defined by the tape command, the PCU transmits the appropriate tape status word as the external interrupt code word using the channel external interrupt capability. If, upon completion of a task, the external interrupt enable is false or the data processor channel is then being used to accomplish another function, the PCU "stacks" the task complete information until the channel is free to be used and the external interrupt enable becomes true.

4.6.3.3 Error Condition Reporting. The following error conditions are detected by the PCU at the time a tape command word is received:

a. command word parity error

Table IV-1

PCU Tape Status Word Format

Bit Position	State	Condition
0	1	Ready and Select Acknowledge Interface Signals True
1	1	Device Connected Interface Signal True
2	1	Write Enable Interface Signal True
3	1	BOT Interface Signal True
4	1	EOT Interface Signal True
5	1	End-of-File (Tape Mark) Sensed Causing Termination of Last Operation
6	1	Tape Parity Error, LRC Error, or CRC Error Detected During Last Operation
7		Spare
8		Spare
9	1	Lost Data/Time Out During Last Operation
10	X	UIO } Unit Select Interface Signals - State of Unit Identification
11	X	UI1 }
12	1	Command Word Conflict - Controller Unable to Perform Operation
13	1	Data Processor Channel Parity Error Detected
14	X	TAO } Tape Number - Absolute Transport Address Bits
15	X	TA1 }

b. command word conflict

When one of these error conditions is detected the PCU will:

a. update the appropriate tape status word;

b. if external interrupts are enabled for the channel on which the command word was received, generate an external interrupt to the IOC on that channel using the updated tape status word as the external interrupt code word;

c. not perform the function requested by the command word.

The following error conditions are detected by the PCU during the tape operation:

a. CRC error

b. LRC error

c. data timeout error

d. data parity errors

When one of these errors is detected the PCU will:

a. update the appropriate tape status word;

b. continue the IOC operation with which the error is associated;

c. if external interrupts are enabled for the channel on which the opertion is being performed, generate an external interrupt on the channel when the I/O operation has completed (i.e., when a SCMT command has been received on the channel). The updated tape status word is used as the external interrupt code word.

4.7 Tape Command Words

Tape command words are issued by the PCU to control MTTU functions. The mnemonics and the commands are as given in Table IV-2 whereas the command word format is as shown in Figure 4.5. All numbers used in the format are binary numbers and must be right adjusted in the respective fields.

COMMAND MNEUMONIC	COMMAND WORD BIT POSITION															
	15	14	13					8	7							0
RRBF	TN (0-3)		0	0	0	0	0	0	Unused							
RRCF	TN		0	0	0	0	0	1	Unused							
RRFM	TN		0	0	0	0	1	0	Unused							
WRBF	TN		0	0	0	0	1	1	Unused							
WMTM	TN		0	0	0	1	0	0	Unused							
SBTS	TN		0	0	0	1	0	1	Unused							
CNGF	TN		0	0	0	1	1	0	U	Number of Gaps (1-127)						
CNGB	TN		0	0	0	1	1	1	U	Number of Gaps (1-127)						
CNMF	TN		0	0	1	0	0	0	U	Number of Marks (1-127)						
CNMB	TN		0	0	1	0	0	1	U	Number of Marks (1-127)						
SCMT	TN		0	0	1	0	1	0	Unused							
REWT	TN		0	0	1	0	1	1	Unused							
SKWF	TN		0	0	1	1	0	0	Key Word							
RTSW	TN		0	0	1	1	0	1	Unused							
LTSW	TN		0	0	1	1	1	0	Unused							S

TN = Tape Number
U = Unused
S = 1 -Select Tape
S = 0 -Deselect Tape

Figure 4.5 PCU MTTU Command Word Formats

Table IV-2

MTTU Command Words

Mnemonic	Command
RRBF	Read Record Block Forward
RRCF	Read Record Continuously Forward
RRFM	Read Record Frame Mode
WRBF	Write Record Block Forward
WMTM	Write Magnetic Tape Mark
SBTS	Skip Bad Tape Spot
CNGF	Count n Gaps Forward
CNGB	Count n Gaps Backward
CNMF	Count n Tape Marks Forward
CNMB	Count n Tape Marks Backward
SCMT	Stop Current Magnetic Tape
REWT	Rewind
SKWF	Search Key Word Forward
RTSW	Read and Clear Tape Status Word
LTSW	Load Tape Select Word

The following contains descriptions of PCU tasks performed for each of the command words. The response to each command word, except when stated otherwise, shall be to initiate tape motion in the direction indicated, perform the commanded operation and, at the completion, update the status word to indicate any errors in the commanded operation and the status of the MTTU used in the operation.

A. RRBF - Read Record Block Forward. This command provides for the transfer of one complete block of data characters for the tape as previously described. Tape motion is stopped in the IBG at the end of the record block.

B. RRCF - Read Record Continuously Forward. This command is identical to RRBF except that read continues until a Stop Current Magnetic Tape (SCMT) command is received or upon detection of a tape mark. Until SCMT is received, block gaps will not result in a stop tape operation. Upon receipt of a tape mark, the read operation is terminated with the tape being positioned in the gap following the tape mark. The tape mark is the last read data transferred to the Data Processor.

C. RRFM - Read Record Frame Mode. This command provides for reading all nine tracks of tape data. Parity checking and character assembly are inhibited and the data from all 9 tape channels are transferred in 9-bit bytes to the Data Processor, including record data, CRC, and LRC, in that order, permitting the establishment of the record image in the Data Processor memory for error correction and data recovery purposes, at the option of the user program. Tape motion is stopped in the IBG at the end of the record block.

D. WRBF - Write Record Block Forward. This command provides for the transfer of one complete block of data characters to the tape as previously described. Tape motion is stopped by a SCMT command.

E. WMTM - Write Magnetic Tape Mark. This command provides for recording the single character tape mark on the tape. Tape motion is stopped in the IBG following the tape mark.

F. SBTS - Skip Bad Tape Spot. This command provides for recording a long interblock gap (3.5 inches) in place of the normal gap. For this command, the extended IBG is recorded and the tape motion is stopped.

G. CNGF, CNGB - Count n Gaps Forward, Backward. These commands provide for moving the tape in the direction indicated past the specified number (n) of interblock gaps. The tape is stopped in the IBG following the nth block. If a tape mark or BOT is sensed before completion of the count, the tape is stopped, and the status word is updated to indicate tape mark, EQT, or BOT.

H. CNMF, CNMB - Count n Tape Marks Forward, Backward. These commands provide for moving the tape in the direction indicated past the specified number (n) of tape marks. The tape is stopped in the IBG following the nth tape mark. If EOT and tape mark or BOT is sensed before completion of the count, the tape is stopped, and the appropriate status bits are set.

I. SCMT - Stop Current Magnetic Tape. This command provides for the termination of the operation in progress on the specified MTTU. If the operation in progress involves read, search, or count operations, the tape continues its

motion until the next IBG is encountered, is stopped in that IBG, and the status word is updated. If the operation in progress involves a write operation, the tape is stopped so as to leave a normal IBG and the status word is updated. This command has no effect on any other operations.

J. REWT - Rewind. This command word provides for rewind of the tape reel to BOT. If a rewind is issued while the tape is at BOT, no tape motion occurs, and the status word is updated to BOT.

K. SKWF - Search Key Word Forward. This command word provides for the examination of the first eight bits of each record block encountered as the tape moves forward. These eight bits are compared for equality to the first eight bits of the command word. If the equality is satisfied, the tape travel is reserved, and the tape is stopped in the IBG prior to the desired eight bits. The search operation continues until equality is found or tape mark is detected, whichever comes first.

L. RTSW - Read Tape Status Word. The PCU will report the status of any tape unit in response to a Read Tape Status Word (RTSW) command referencing that tape unit. Upon receiving such a command, the PCU will transmit the specified tape status word to the IOC via the external interrupt capability of the tape channel on which the RTSW command was received. As is always the case, the transfer of status in response to an RTSW command will occur only if external interrupts are enabled on the tape channel to be used.

M. LTSW - Load Tape Select Word. This command defines which tape select request signals are to be set.

4.8 Programming for Tape Operations

4.8.1 Preparations for Read or Write Operations

4.8.1.1 External Interrupt Enabling. It is necessary to enable external interrupts to receive notification of tape task completion (see Section 4.6.3.2) and to allow for notification of error conditions. Error conditions associated with a tape operation may be detected by the PCU either upon receiving a command requesting initiation of the operation (e.g., command word parity

error) or during the transfer of data words for the operation (e.g., data parity error, data timeout error). If a report of any error condition which may arise associated with the tape operation is desired, external interrupts should be enabled on the channel to be used for the operation prior to initiation of the operation.

Example:

Execution of the following IOC instruction chain enables an external interrupt to occur on channel 11 of the IOC executing the chain:

```
EIEM     XB     11,     EIBCW,     3,   0,   1

EIBCW    BCW    EIBUF,  1    . Buffer Control Word

EIBUF    RES    1
```

The XB (Initiated External Interrupt Buffer) instruction permits an external interrupt to occur on channel 11 and initiates a one-word buffer in main memory for input of a tape status word in the event of an external interrupt. The buffer control word at address EIBCW specifies that the tape status word transmitted as the external interrupt code word will be loaded into the one-word buffer at main memory address EIBUF. The k-field specifies that the 16-bit status word will be loaded into bits 15-0 of the location EIBUF. The c-field specifies that the XB instruction is the last instruction in the chain. The m-field specifies that a class 3 monitor interrupt is to be generated to the CPU in the event of an external interrupt on channel 11.

4.8.1.2 Tape Unit Selection. Having enabled interrupts on channel 11, one can now proceed to select the tape unit to be used with assurance that should an error be encountered it would not go unreported.

Example:

Execution of the following IOC instruction chain selects tape unit 2, rewinds the tape and transfers the task complete status word.

```
                  j     y      k    c    m

INIT     FB       11,  LTSW,  1,   1,   0
```

```
        FB      11,  REWT,   1,   0,   0

LTSW    +0107001 . Select tape unit 2

REWT    +0105400 . Rewind tape unit 2
```

Each of the two FB instructions in this chain issues one command word to the PCU on channel 11. Each of these commands is issued without force (k=1), and no monitor interrupts are requested following transfer of any of the commands (m=0). The first FB instruction issues a Load Tape Select Word command directing the PCU to issue a selection request to tape unit 2. The second FB instruction issues a Rewind command directing the PCU to rewind tape unit 2.

4.8.1.3 Backspace. Should it not be desired to return a tape to BOT before reading or writing, the option exists to backspace a specified number of IBGs.

Example:

The following example backspaces the tape on unit 0 ten blocks (IBGs) and transmits task completion.

```
                j      y     k   c   m

BACKSP  FB    11,   CNGB,   1,  0,  0

CNGB    +03412 . Count 10 tape marks backwards on tape unit 0.
```

4.8.2 Read and Write Operations

When the preliminary tasks described above have been accomplished, the desired tape operation can be performed. A simple tape operation can be accomplished with a single IOC instruction chain of the following general form:

FB (without force) to issue a tape control command (RRBF, RRCF, RRFM or WRBF) to the PCU to initiate the operation.

OB (or IB) to initiate the transfer of data words to or from memory.

FB (with force) to issue a tape control command (SCMT) to PCU to stop the operation.

The first FB instruction directs the IOC to initiate the output of one word as a command to the PCU. This command is sent to the PCU on the tape data transfer channel referenced by the FB instruction and it is sent without force. From the information contained in this command word, the PCU identifies the tape unit to be used for the operation. The PCU then initiates the requested tape operation. The channel on which the command word was received by the PCU is the channel on which the PCU requests or sends data words to the IOC during the operation.

An OB instruction directs the IOC to initiate the output of data words from memory to the PCU on the tape data transfer channel referenced by the OB instruction. The buffer control word referenced by the OB instruction defines the number of words to be output and the location of the main memory buffer from which they are to be output. An IB instruction directs the IOC to initiate the input of data words from the PCU on the tape data transfer channel referenced by the IB instruction. The buffer control word referenced by the IB instruction defines the number of words to be input and the location of the main memory buffer to which they are to be input. The OB or IB instruction must reference the same channel referenced by the initial FB instruction.

During the input/output operation, the IOC keeps track of the number of words to be transferred (as specified by the buffer control word referenced by the IB or OB instruction). When transfer of the last data word has been completed, the IOC executes the next instruction, which may or may not be a SCMT instruction (some instructions by their definition contain a built in "stop" command, e.g., RRBF).

In the four examples that follow, external interrupts have been enabled (as in the example of Section 4.8.1.1) prior to entering the READ or WRITE routine. In addition, the three READ examples involve tapes that have been written on with 96-word records.

4.8.2.1 Read Operation Number One. Execution of the following IOC chain results in the transfer of one 96-word (16 bits) block from tape unit one followed by the transmission of task completion.

```
                    j       y       k     c     m
READ      FB    13,     RRBF,    1,    1,    0
          IB    13,     RDBCW,   3,    0,    0
```

```
RRBF    +040000 . Read record block forward

RDBCW   BCW  RDBUF, 96 . Buffer control word for input buffer

RDBUF   RES  96  .96 word input buffer
```

4.8.2.2 Read Operation Number Two. The following routine transfers two complete records with the one RRCF command, stops the tape and transmits a tape complete status word.

```
                j      y      k    c    m

READC     FB   13,   RRCF,   1,   1,   0

          IB   13,   RDBCW,  3,   1,   0

          FB   13,   SCMT,   0,   0,   0

RRCF    +040400 . Read record continuously forward

RDBCW   BCW   RDBUF, 192

RDBUF   RES   192

SCMT    +045000 . Stop command
```

4.8.2.3 Read Operation Number Three. The Read Record Frame Mode (RRFM) allows for data recovery after detection of an error condition (see Section 4.7 for details). The following routine transfers to the memory of the AN/UYK-7 the record image of the tape (192 nine-bit words plus CRC and LRC). Figure 4.6 illustrates the connection between the data recorded on the tape and the data stored in the memory of the AN/UYK-7. Appropriate software allows for the isolation of multiple errors.

```
                j      y       k    c    m

READF     FB   13,   RRFM,    1,   1,   0

          IB   13,   RDBCW,   3,   0,   0

RRFM    +041000

RDBCW     BCW      RDBUF, 194

RDBUF     RES      194
```

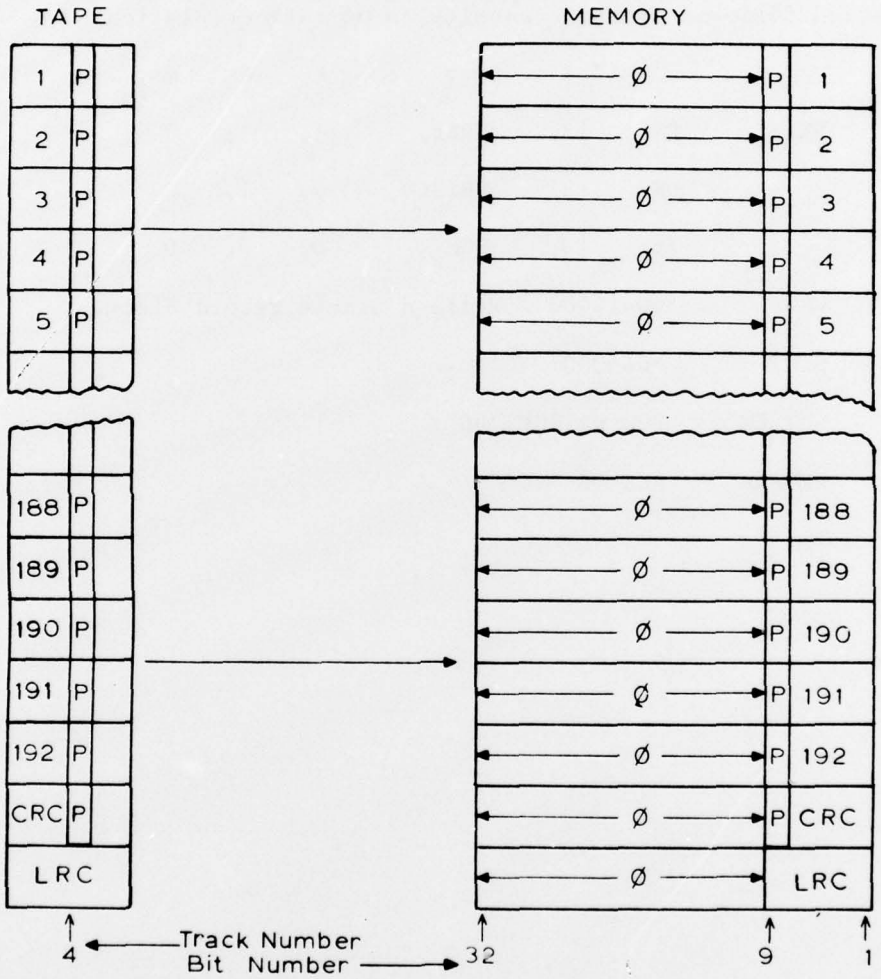


FIGURE 4.6. THE MAPPING OF 96(16-BIT) WORDS FROM THE SMSS TO MAIN MEMORY IN RESPONSE TO A READ RECORD FRAME MODE (RRFM) COMMAND. THE NUMBERS IDENTIFY THE 192 HALF-WORDS.

4.8.2.4 A Write Operation. Execution of the following IOC instruction chain results in the transfer of a 96 word (16 bits) record to the tape on tape unit 1 followed by termination of tape motion followed by the transmission of task completion.

```
                    j       y         k    c    m
WRITE     FB    13,     WRBF,      1,   1,   0
          OB    13,     WRTBCW,    3,   1,   0
          FB    13,     SCMT,      0,   0,   0
WRBF      +0410400 . Write a single record block.
SCMT      +045000
WRTBCW    BCW WRTBUF, 96
WRTBUF    RES 96
```

APPENDIX A

THE PRIMARY MASS STORAGE SUBSYSTEM

FUNCTIONAL CHARACTERISTICS OF A PMSU

- PROVIDES UP TO TWO DISKS (PMSDs) (MU-626/T) EACH WITH THE FOLLOWING CHARACTERISTICS
  - 100 TRACKS
  - 3936 16-BIT WORDS/TRACK
  - 2000 RPM
  - FIXED HEADS
  - MAXIMUM 1 REVOLUTION ACCESS TIME
- PROVIDES INTERFACE BETWEEN UP TO TWO CONTROLLERS AND DISK(S)
- PROVIDES SELECTION OF WHICH CONTROLLER GAINS ACCESS TO DISKS

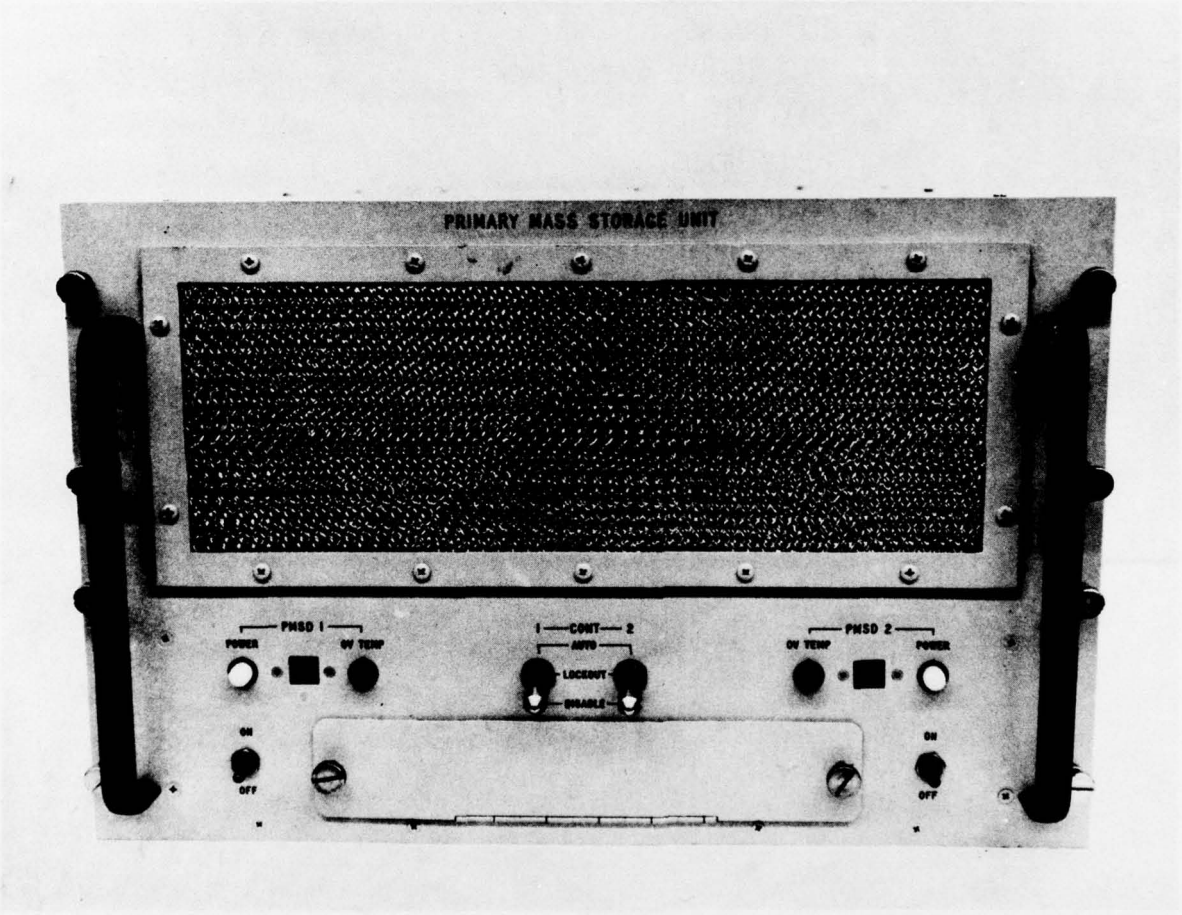


FIGURE A.1. A PRIMARY MASS STORAGE UNIT

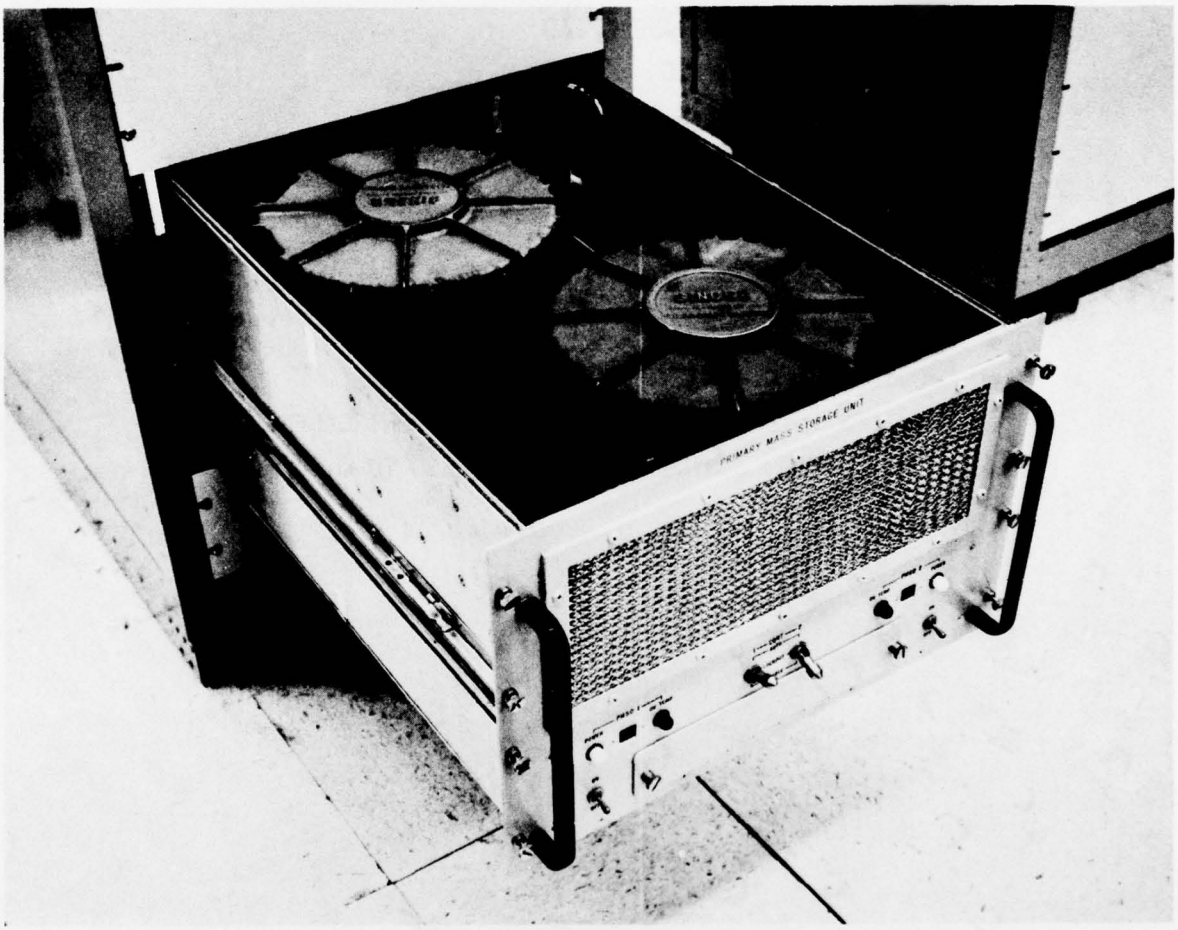


FIGURE A.2. A PRIMARY MASS STORAGE UNIT EXPOSED TO REVEAL TWO PRIMARY MASS STORAGE DEVICES.

APPENDIX B

THE SECONDARY MASS STORAGE SUBSYSTEM

FUNCTIONAL CHARACTERISTICS

MTTU (UNIVAC 1840)

- 75 IPS READ/WRITE TAPE SPEED
- 150 IPS REWIND SPEED
- 9 TRACKS - 800 BITS PER INCH
- ACCEPTS STANDARD 10.5" REEL - 1/2" TAPE
- INDUSTRY COMPATIBLE FORMAT

DIOU

- PROVIDES OPERATIONAL INDICATORS (LOAD POINT, READY, ETC.)
- PROVIDES SWITCHES FOR LOCAL CONTROL MODE
- PROVIDES REMOTE MODE FOR COMPUTER CONTROL
- PROVIDES INTERFACE BETWEEN MTTU & 2 CONTROLLERS
- SELECTS WHICH CONTROLLER GAINS ACCESS TO MTTU

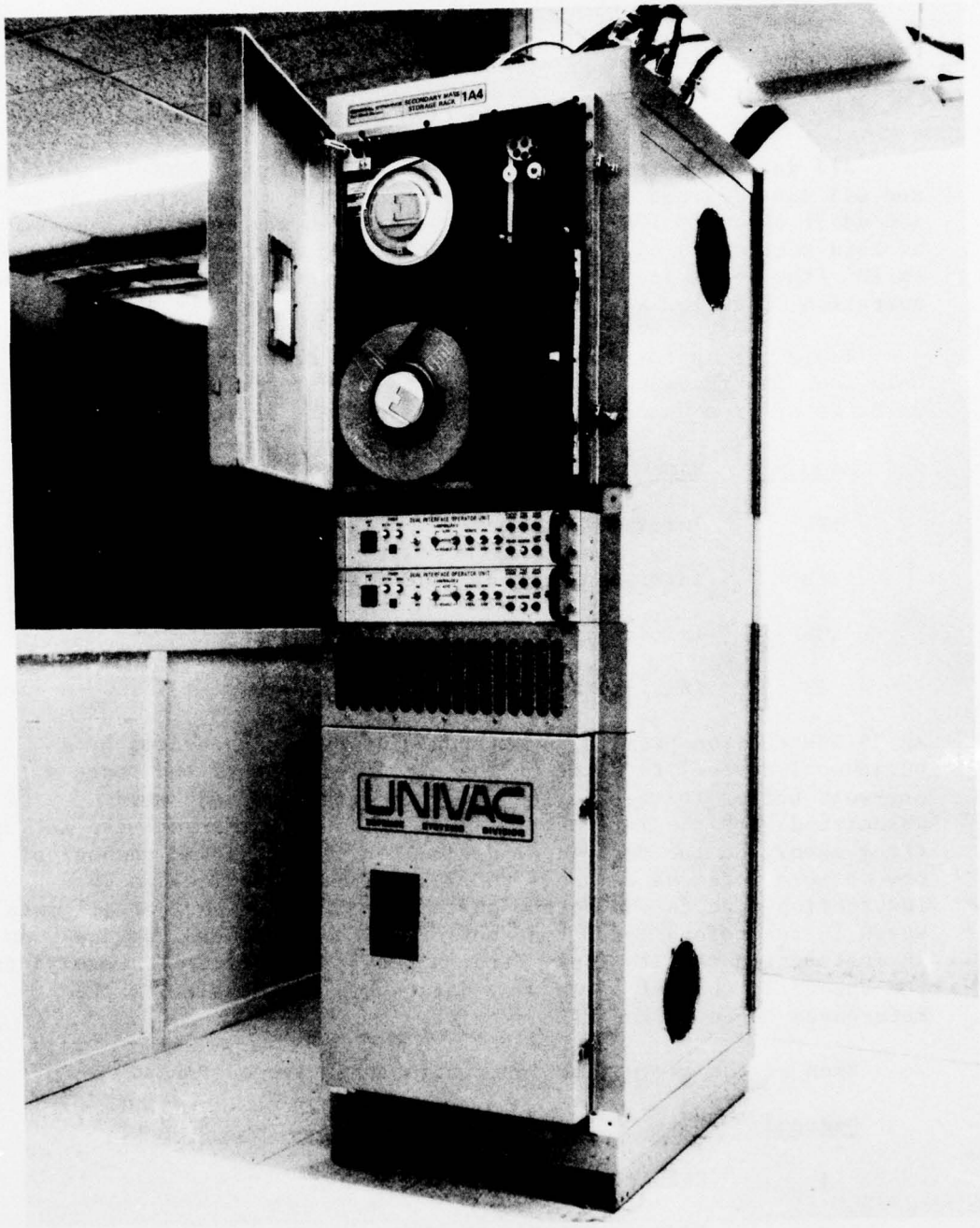


Figure B.1. Two MTTUs and Two DIOUS Mounted in a Secondary Mass Storage Rack.

APPENDIX C

IOC Instruction Chains

All data transfers between the memory of the AN/UYK-7 computer and all input/output devices are performed under the control of an IOC as it executes IOC instructions stored in memory. The purpose of this section is to familiarize the reader with the programming of an IOC (the construction of chains of IOC instructions) and with the operation of an IOC as it executes its instructions.

There are approximately two dozen different IOC instructions. Only four instructions which direct the transfer of one or more words to or from memory will be discussed here as follows:

Mnemonic	Name
XB	Initiate External Interrupt Buffer on Channel j
FB	Initiate External Function Buffer on Channel j
OB	Initiate Output Buffer on Channel j
IB	Initiate Input Buffer on Channel j

An XB instruction permits an external interrupt (generated by a peripheral device) to occur on the specified channel and opens a one-word buffer to receive the external interrupt code word associated with the interrupt. An FB instruction directs the output (from memory to the peripheral device) on the specified channel of one or more words as commands to the peripheral device. An OB instruction directs the output on the specified channel of all data words in the referenced output buffer to the peripheral device. An IB instruction permits input (from a peripheral device to memory) on the specified channel of as many data words as the size of the referenced input buffer will permit.

Each of the above four instruction has five operands:

Operand	Name
j	Channel (0 : value : 15)
y	Address (18-bit absolute address)
k	Parameter (0 : value : 3)

c	Chain bit (0 or 1)
m	Monitor bit (0 or 1)

For each of the instructions the j-operand identifies the channel on which data transfer is to occur.

The y-operand specifies the location of the data to be transferred. In an FB instruction (with k=0 or 1), y is the address of the one word I/O device command to be transferred. In an XB, OB, IB, or FB instruction (with K=2), y is the address of a buffer control word (BCW) which specifies the initial and final addresses of a buffer. This buffer contains the words to be transferred upon output and contains the locations to be loaded upon input.

For the FB instruction, the k-operand identifies the mode of the transfer:

FB Instruction

k	Meaning
0	Transfer one word with force
1	Transfer one word when requested (by the peripheral device)
2	Transfer many words as requested (by the peripheral device)

In the case of FB instruction, when k equals zero, data transfer occurs when the instruction is being executed without waiting for a data transfer request from the peripheral device. For the other three instructions, the k-operand specifies the word fraction which is to be transmitted upon each data transfer:

XB, OB, IB Instructions

k	Meaning
0	Transfer no data (data suppression)
1	Transfer one-quarter word (8 bits)
2	Transfer one-half word (16 bits)

3 Transfer a full word (32 bits)

If the c-operand (chain bit) is set to one, then upon completion of the execution of the current IOC instruction, the IOC will retrieve the word from the next sucessive location in memory (after the address from which the current instruction was retrieved) and proceed to execute it (instruction chaining). If the c-operand is set to zero, no further IOC activity will occur after completion of the execution of the current instruction (end of a chain).

If the m-operand (monitor bit) is set to one, then upon completion of the execution of the current IOC instruction, the IOC will generate a Class 3 monitor interrupt. The interrupt status code (ISC) associated with the interrupt will identify the interrupting IOC, the interrupting channel (the value of the j-operand in the IOC command) and the type of the interrupt (whether the IOC instruction was XB, FB, OB or IB). If the m-operand in the IOC instruction is set to zero, no monitor interrupt will be generated.

Thus, an example of an IOC chain is:

FB Channel=14, address of command(1), k=1, c=1, m=1

OB Channel 14, address of BCW(1), k=3, c=1, m=1

FB Channel=14, address of command(2), k=0, c=0, m=1

In this case, three IOC instructions will be executed where each instruction specifies data transfers which are to occur on channel 14. The values of the chain bit in the three instructions link the first to the second, the second to the third, and shows that the third instruction is the end of the chain. The monitor bits indicate that a monitor interrupt is to be generated upon the completion of each command. The k-operands and address operands declare that:

1. Command(1) is to be sent as soon as the peripheral device on Channel 14 requests a command word transfer.

2. A full word data transfer is to be made for each word located within the buffer specified by BCW(1).

3. Command(2) is to be sent with force (as soon as the OB command has been completed and the second FB instruction is executing).

Note that if BCW(1) specifies a buffer size of 100 words, execution of this IOC chain will result in 102 single word data transfers with an FB monitor interrupt being generated after the first word transfers, an OB monitor interrupt after 101 words have been transferred, and an FB interrupt after the last word has been transferred.

The execution by a given IOC of an IOC instruction chain which starts at a given address is initiated by any CPU program executing an Initiate I/O instruction which references the given IOC and the starting address of the chain. The execution of any IOC instruction chain is terminated upon the completion of the execution of any IOC instruction in the chain in which the chain bit is equal to zero.

REFERENCES

1. Sperry Rand-UNIVAC, AN/UYK-7 Military Computer Technical Description, Unclassified.

2. Sperry Rand-UNIVAC Technical Memorandum, Document NS 1973TR0002, AN/UYK-7 Input/Output Operation, Unclassified, 1 March 1973.

3. Sperry Rand-UNIVAC, AN/UYK-7 Assembler Programmer's Reference/User's Manual, Unclassified, April 1974.

4. Sperry Rand-UNIVAC, Technical Manual: Magnetic Tape Transport and Remote Operator Unit, Vol. I (PX-8122-1-3), September 1976.

SUPPLEMENTARY DOCUMENTS

- Specification CP-4850114-A, Prime Item Specification for the CP-1201(V)/UYK-25(V) Processor, General Purpose Digital (Peripheral Controller Unit), 17 August 1976.

- Specification CP-4850132-A, The C-9852/T Control-Power Supply, Tape Drive (Dual Interface Operator Unit).